DEPARTMENT

OF INFORMATION ENGINEERING

Large-Bandwidth Triple-Loop Control of Grid-Connected Inverters

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1. Abstract

A large-bandwidth, triple-loop controller designed for single-phase, grid-tied inverters is analyzed. This organization provides several benefits, including a regulated local ac voltage, a largebandwidth control of the injecting power and a good robustness against different types of grid perturbations. Besides, the proposed controller is inherently able to guarantee seamless transitions between grid-tied and islanded operation, showing good potential for application to nano- and microgrid utility interface converters.

3. Control strategy

• Inductor current loop (deadbeat controller) provides satisfying system damping and rapid overcurrent protection.

 Output voltage loop(deadbeat controller) guarantees seamless mode transitions and highquality local-voltage supply.

· Grid current loop (PI controller) can be designed with relatively large bandwidth. This is crucial to attain good harmonic attenuation and resilience to grid perturbations.

5. Achieved advantages

- excellent reference tracking performance.
- · a strong attenuation of converter-side and grid-side harmonics.
- · grid-connected and islanded operations and seamless transitions between the two.
- · robust stability in the presence of grid perturbations (grid voltage harmonic pollution, amplitude and frequency fluctuations or connection impedance parameter variations).

7. Experimental verification



8. Future work

- Auto-tuning of the grid current loop.
- Top level control scheme of the hybrid AC/DC micro grid.

2. System configuration



Structure of labVIEW - FPGA program

User Interface VI

PCI bu

Real-Time VI

Real-Time Processor

1 Ethernet

FPGA VI

FPGA

4. Large-bandwidth triple-loop controller



Structure of the proposed triple-loop controller

Host PC - labVIEW

NI cRIO-9068

Ethernet

6. Implementation of the proposed controller

Control equations of each loop:

$$\begin{split} d &= \frac{L f_{sw}}{V_{DC}} \cdot \left[i_L^{REF} - i_L \right] + \frac{v_O}{2V_{DC}} + \frac{1}{2}. \ \ (1) \\ i_L^{REF} &= C_O f_{sw} \cdot \left[v_O^{REF} - v_O \right] + i_O, \ \ \ (2) \\ v_O^{REF} &= H_{PI} \cdot \left(i_G^{REF} - i_G \right). \end{split}$$



access and integrate all the components of the cRIO; provides the operator with graphical human machine interface(HMI).

Real-Time processor:

provides reliable, predictable behaviour and excels at floating-point math and analysis.

• FPGA:

excels at high-speed logic and precise timing.



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