Organisational Information

Sign up at: www.ecpe.org/events

Registration Deadline:
6 November 2024

Participation Fee:

€ 670,– *	for industry
€ 520,– *	for universities/institutes
€ 180,– *	for students/PhD student (limited spaces; copy of students ID required)
€ 120,– *	participation 3rd day for industry
€ 100,– *	participation 3rd day for university

* plus VAT

- The participation fee includes dinner, lunches, coffee/soft drinks and digital proceedings. The reduced (PhD) students fee includes all except for dinner (can be booked for an extra fee of € 50,-*)
- Digital proceedings will be provided by download link latest one day before start of the event. A printed handout is available on request (€ 50,-*).
- Upon receipt of registration confirmation via email you are signed-up for the event. The invoice will be sent via email.
- 25 % discount for participants from ECPE member companies.
- 10% discount on university/institute fee for participants from ECPE competence centres.
- Further information (hotel list and maps) will be provided after registration and can be found on the ECPE web page.
- Cancellation policy: Full amount will be refunded in case of cancellation upon to 2 weeks prior to the event. After this date 50 % of the fee is non-refundable (replacement is possible).

12/11/24

Organisational Information

Organiser	ECPE e.V. 90443 Nuremberg, Germany www.ecpe.org
Technical Chair	Dr. Reinhold Bayerer Physics of Power Electronics (D)
Technical Contact	Thomas Harder, ECPE e.V. +49 911 81 02 88 – 11 Thomas.harder@ecpe.org
Organisation	Marietta Di Dio, ECPE e.V. +49 911 81 02 88 – 13 Marietta.didio@ecpe.org
Venue	OREA Hotel Angelo Praha Radlická 3216/1g 150 00 Praha 5 Czech Republic

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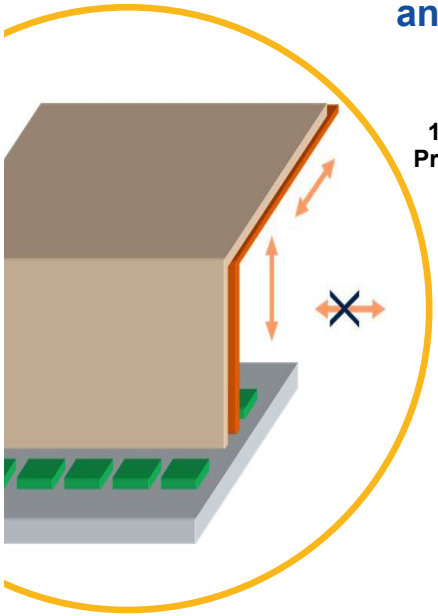
European Center for Power Electronics e.V.

ECPE Tutorial

Power Circuits for Clean Switching and Low Losses



13 - 14 November 2024
Prague, Czech Republic

ECPE Tutorial

Power Circuits for Clean Switching and Low Losses

13 - 14 November 2024
Praha, Czech Republic

This tutorial will teach the various effects of parasitic inductance (L_S) in power electronics. As power density and current density is continuously growing, parasitic inductance and resistance become limiting factors, more and more. The use of unipolar devices, e.g. WBG-devices, requires minimum parasitic inductance to allow fast switching. The figure of merit is the product of parasitic inductance times rated current (L_S*I_{nom}) which is increasing with current density, if designs do not improve.

Not only overvoltage during turn-off is the problem but for bipolar power semiconductors like IGBTs and freewheeling diodes, parasitic inductance causes disadvantageous current waveforms.

In systems, which have snubber capacitors additional to the DC-link capacitor and parasitic inductance in between, oscillations between these capacitors occur.

When considering power semiconductors, in parallel, current sharing of voltage-controlled devices like IGBT, MOSFET and JFET can be affected by the presence of even very small parasitic inductance. Parasitic inductance within the control circuit (gate circuit) decouples driver and Gates of the devices, leading to increased short circuit current, for example.

To introduce these topics the tutorial will start with the basics of switching inductive loads and discussion of related waveforms. Investigations on the different effects, as well as related power semiconductor physics, will follow. The discussion of paralleling will be accompanied by case studies. Geometries of conductors and system design for low parasitic inductance and good current sharing will be another main part and the conclusions will summarize the benefits of related system design – clean switching and low losses.

Participants can contribute to the tutorial by own examples or problems in their power circuits. Given circuit designs or waveforms as taken from power circuits will be discussed. If participants are able to supply such examples, an online meeting will be arranged, two weeks after the tutorial on November 29. Details will be given during the tutorial.

The tutorial is chaired by:

Dr. Reinhold Bayerer, Physics of Power Electronics
Prof. Thomas Basler, Chemnitz University of Technology

All presentations and discussions will be in English.

Programme

Wednesday, 13 November 2024

09:00	**Registration & Welcome Coffee**
09:30	**Welcome** ECPE e.V.
09:45	**Power Semiconductors Switching Inductive Load and Parasitic Inductance** Reinhold Bayerer
10:45	**Geometry of Conductors and Their Inductance – Determination and Evaluation** Reinhold Bayerer
12:05	**Lunch**
13:05	**Parasitic Inductance Meets Parasitic Resistance** Reinhold Bayerer
13:20	**Parasitic Inductance – Effecting Switching Characteristics and Stress Factors of Power Semiconductors** Reinhold Bayerer
13:50	**Turn-off Behavior of Bipolar Devices – IGBT and Diode: Influence of DC-Voltage, Current and Gate Control** Thomas Basler
14:35	**Break**
14:55	**Turn-off Behavior of Bipolar Devices – IGBT and Diode: Influence of DC-Voltage, Current and Gate Control** Thomas Basler
16:15	**Clean Switching of WBG Devices** Thomas Basler
18:00	**End of 1st Day**
19:00	**Dinner**

Programme

Thursday, 14 November 2024

08:30	**Start of 2nd Day**
08:30	**Parasitic Inductance – Effecting System Losses incl. EON/EOFF-Dependence on Ls** Reinhold Bayerer
10:00	**Parasitic Inductance – Effecting Current Sharing of Paralleled Power Devices** Reinhold Bayerer
10:35	**Break**
10:55	**Case Study I: Asymmetric Paralleling and Discussion** Reinhold Bayerer
11:25	**Case Study II: Asymmetric Paralleling and Discussion** Reinhold Bayerer
11:45	**Gate Inductance** Reinhold Bayerer
12:25	**Lunch**
13:25	**Oscillations in DC-Bus incl. SiC** Reinhold Bayerer
14:35	**Measuring Challenges and Solutions** Reinhold Bayerer
14:55	**Break**
15:15	**Examples of Discretes on PCB** Reinhold Bayerer
16:05	**Final Discussion and Planning Extra Day**
16:35	**End of Tutorial**

2 weeks later, 27 November 2024 - online

Extra Day for Discussion Examples or Problems Supplied by Participants (online)
Reinhold Bayerer