ECPE Guideline PSRRA 01

Railway Applications

HV-H3TRB tests for Power Semiconductor

Release no.: 03.02/2024

Release date: 20.02.2024

Contact: ECPE European Center for Power Electronics e.V.
Dr. Chris Gould
Landgrabenstrasse 94
90443 Nuremberg, Germany
Email chris.gould@ecpe.org
Phone (+49) 911 8102 880

ECPE Working Group
Power Semiconductor Reliability for Railway Application - PSRRA

Preface

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Contents

1 Scope

This document describes a steady-state temperature, humidity and voltage bias test for the evaluation of the behavior of non-hermetically sealed power electronic IGBT and SiC MOSFET modules for the use in rolling stock applications.

2 Normative references

Standard	Date of Issue	Title
IEC 60749-5	2017-04	Semiconductor devices – Mechanical and climatic test methods – Part 5: Steady-state temperature humidity bias test
IEC 60068-2-67	1995	Environmental testing – Part 2-67: Tests – Test Cy: Damp heat, steady state, accelerated test primarily intended for components
IEC 60747-9	2007-09	Semiconductor devices – Discrete devices – Part 9: Insulated-gate bipolar transistor (IGBTs)
IEC 60747-2	2016-04-13	Semiconductor devices - Part 2: Discrete devices - Rectifier diodes
IEC 60747-15	2010-12-16	Semiconductor devices - Discrete devices - Part 15: Isolated power semiconductor devices
IEC 62497-2	2010-02-18	Railway applications — Insulation coordination Part 2: Overvoltages and related protection

3 Abbreviations

DS	Datasheet
T_a	Ambient temperature
T_{vjmax}	Maximum virtual junction operation temperature
$T_{vj\_initial}$	T_{vj} at the starting phase of the test
R_{THja}	Thermal resistivity between junction and ambient
V_{ISO}	Isolation test voltage
V_{bias}	Applied V_{CES} test voltage
V_{CES}	Collector-Emitter voltage with Gate-Emitter short-circuited
V_{DSS}	Drain-Source voltage with Gate-Source short-circuited
U_{max1}	Highest permanent DC catenary voltage
U_{max2}	Highest non-permanent DC catenary voltage
U_{max3}	Highest temporary Over-voltages
V_{CEsat}	Collector-Emitter saturation voltage of IGBT
$R_{DS(on)}$	Drain-Source on-resistance of MOSFETs
V_F	Forward voltage drop of Diode

V_{SD}	Forward voltage of the internal body diode (corresponds to the voltage of the Drain-Source path in reverse operation)
$V_{GE,th}$	Gate-Emitter threshold voltage of IGBT
$V_{GS,th}$	Gate-Source threshold voltage
I_{CES}	Collector-Emitter cut-off current, Gate-Emitter short-circuited
I_{GES}	Gate leakage current, Collector-Emitter short-circuited
I_{DSS}	Drain-Source leakage current
I_{GSS}	Gate-Source leakage current

4 Definitions

4.1 HV-H3TRB-Test

HV-H3TRB is conducted in a same/similar way as the IEC60068-2-67 and IEC 60749-5 standard, with the addition of clearly defining the test voltage to be applied in relation of the device voltage class.

4.2 Voltage classes:

The test is applicable for the standard IGBT and SiC MOSFET power module voltage classes for rolling stock applications, ranging up to 6500 V.

5 General conditions

The general test conditions are as defined in the IEC60068-2-67 and IEC 60749-5 standards. Specifically, the standard test temperature and relative humidity are set to 85°C and 85%. The ramp-up, the ramp-down, the drying and the test durations are defined separately in this document.

The following definition shows typical number of test devices with new chip design and new packages. The use of generic “family data” to simplify the qualification process is accepted.

Recommended number of samples:

Criteria	Sample number
Min. number of modules	9
Min. number of modules per lot	3
Min. number of module prod. lots	3
Min. number of chips	72 transistors (IGBTs or MOSFETs) and diodes each
Min. number of chip prod. lots	3

6 Test requirements for the HV-H3TRB

6.1 Definition of test voltages

The test voltage is not regarded as acceleration factor for the test. Thus, the test voltage is selected in the range of the typical use case and defined dependent on the voltage class. In general, the test voltage is defined to fulfill the requirements of U_{max2} for 750 V, 1500 V and 3000 V catenary voltages according to IEC 62497-2, table A.1 – Overvoltages. This is reached by setting V_{bias} at approximately 60% x V_{CES} respectively V_{DSS}.

As an exception to this rule, 3000 V is set as test voltage for 4500 V devices. DC link voltage for applications using 4.5 kV semiconductors is set between 2200 V and 3000 V. DC link with certain tolerance of the control chain has to be considered.

Table 1: Summary of the test voltage for the typical voltage classes of power modules for traction applications and the maximum voltages from IEC 62497-2

Voltage class of power modules	1700 V	3300 V	4500 V	6500 V
HV-H3TRB Test voltage Minimum test voltage	1000 V	1950 V	3000 V	3900 V
Nominal line voltage U_n	750 V	1500 V	-	3000 V
Highest permanent DC catenary voltage U_{max1}	900 V	1800 V	-	3600 V
Highest non-permanent DC catenary voltage U_{max2}	1000 V	1950 V	-	3900 V
Highest temporary Over-voltages U_{max3}	1270 V	2540 V	-	5075 V

6.2 Definition of test temperature

The test temperature is defined as the ambient temperature in the test chamber and shall be set to 85°C. The tolerance for the temperature is ±2° according to IEC 60068-2-67.

If the difference between T_a and $T_{vj\_initial}$ is > 10 K → Action to reduce Delta T below 10 K shall be considered. Potential measures can be the reduction of R_{THja} and / or reduction of mean losses by application of cycled biased voltage. The test clock runs between ramp-up and ramp-down and only when voltage is applied.

Changes in the test control strategy in order to control the junction temperature has to be monitored and protocolled.

6.3 Definition of test humidity

The test humidity is defined as the relative humidity in the test chamber.

The test humidity shall be set to 85%. The tolerance for the humidity is ±5% according to IEC 60068-2-67.

6.4 Acceptance criteria

The acceptance criteria are split in two parts, the in-test and the post-test criteria.

The “in-test” means during the test, the “post-test” after the test. The sampling rate for in-test shall be minimum once per hour.

The **in-test acceptance** criteria

I_{CES} < 10 x $I_{CES\_initial}$ respectively I_{DSS} < 10 x $I_{DSS\_initial}$ (initial leakage current measured after stabilization of the test @V_{bias}). In addition, values under 100 µA are to be considered as below the measurement resolution. Initial leakage currents below 100 µA should be considered as 100 µA.

No breakdown of voltage $V_{CES.}$ respectively V_{DSS}.

The **post-test acceptance** criteria are described in Table 2

Prior to HV-H3TRB test an initial characterization has to be done that includes all parameters according to Table 2.

Room temperature post characterization tests shall be performed before any test at higher temperature. The following table summarizes the acceptance criteria after the HV-H3TRB test.

Table 2: Post-test acceptance criteria

Value	Test temperature	Acceptance criteria
V_F / V_{SD}	room temperature	within DS-limits AND drift <10%
V_{CEsat} / $R_{DS(on)}$	room temperature	within DS-limits AND drift <10%
$V_{GE,th}$ / $V_{GS,th}$	room temperature	within DS-limits AND drift <10%
I_{CES} / I_{DSS}*	room temperature	within DS-limits AND drift <x10*
I_{GES} / I_{GSS}*	room temperature	within DS-limits AND drift <x10*
V_{ISO} *minimum*	room temperature	80% of V_{ISO}

* I_{CES} / I_{DSS} values below 100 µA and I_{GES} / I_{GSS} below 100 nA are to be considered as below the measurement resolution. Initial leakage currents below 100 µA or 100 nA should be respectively considered as 100 µA (or 100 nA).

In case drift criteria are not met but devices are still within specified limits a risk release is possible by proving that functionality under operation conditions is still given as depicted in Figure 1 below:

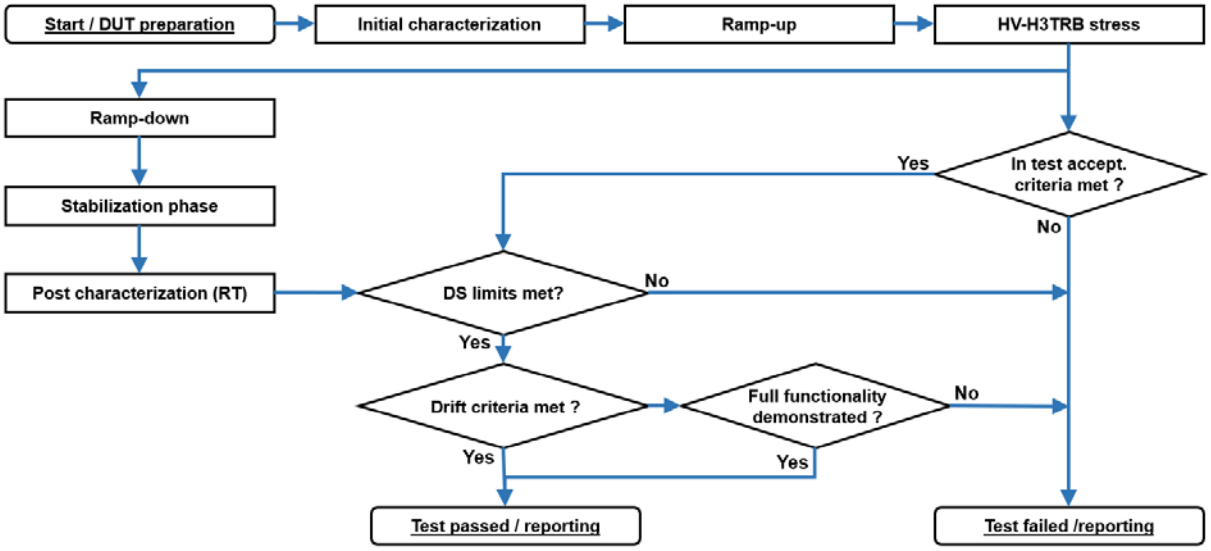

Figure 1: Test and assessment flow-chart (at all decision points pass decision is only possible if all samples pass)

6.5 Test duration

Test duration under voltage shall be 1000 (+168/-24) hours. As alternative, end-of-life (EOL) testing is also allowed and recommended for new technologies up to 2000 hours as maximum test duration.

Final qualification shall be done in 1 run without intermediate readouts in order to avoid reduction of test stress by retarded humidity intrusion.

6.6 Ramp-up

The procedure as defined in chapter 7 of IEC 60749-05 applies. The time to reach stable temperature and relative humidity conditions should be less than 3 hours. Condensation shall be avoided by ensuring that the test chamber (dry bulb) temperature exceeds the wet-bulb temperature at all times.

6.7 Ramp-down

The procedure as defined in chapter 7 of IEC 60749-05 applies. Ramp-down to stabilization condition should not exceed 3 hours. Condensation shall be avoided by ensuring that the test chamber (dry bulb) temperature exceeds the wet-bulb temperature at all times.

6.8 Stabilization phase after the test

The drying process should be defined for each product. The objective is to get humidity sensitive parameters independent of the captured humidity. The drying process conditions shall be kept unchanged for each product.

The preferred procedure is defined in chapter 7 of IEC 60749-05 with modifications based on the specifics of IGBT power modules. An electrical test shall be performed not later than 48 hours after the end of ramp-down which shall include at minimum testing of reverse blocking current and reverse blocking voltage. Within this time window drying by tempering is allowed if room temperature storage is not sufficient to dry out excessive humidity. A deviation of this baseline procedure shall be documented and reasoned in the procurement document.

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