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Internship proposal (6 months)

Design and conception of a smart gate driver for reduced dead-time operation

(reference JLL-03-2022)

Internship supervisors

Mitsubishi Electric R&D Centre Europe **:** Johan LE LESLE, Researcher, Power Electronic System (PES) division, Design and Integration Technologies (DIT) team.

Overall context

Mitsubishi Electric R&D Centre Europe (MERCE) is the European R&D center from the Corporate R&D organization of Mitsubishi Electric. The aim of our center is to provide advanced R&D support to the Japanese R&D centers and to the business units of Mitsubishi Electric Corporation.

Located at the heart of Europe's leading R&D community, MERCE includes two entities: MERCE-France and MERCE-UK. MERCE conducts R&D into next generation communication systems and technologies related to Energy and Environment. Design of next generation power converter is a major activity in the Power Electronic System division (PES), being part of MERCE-France.

Internship subject

The Design & Integration Technology (DIT) team is actively working on advanced packaging in power electronics and optimal design techniques, one of the targets being high-density converters. To reduce the size of the passive components, operate at high switching frequency is a must. Nevertheless, it also comes with an increase in the switching losses. Indeed, the losses generated during the dead-time and due to the body diode conduction cannot be neglected anymore. Therefore, it makes sense to investigate a smart gate driver making possible operations with minimized dead-times.

The internship will be structured around two main tasks: On one hand, a comprehensive literature review on power electronics and the impact of dead times on losses has to be carried out. The bibliographic study will identify some of the most suitable methods and highlight not only the advantages and limitations of each technique but also its applicability to highly integrated power converter. One the other hand, an existing concept at MERCE requires to be further investigated, the bottlenecks still have to be identified and addressed. The investigation on the smart gate driver will be conducted using simulation tools, typically Spice environment. A design procedure is expected for further development. In a second time of the internship, a prototype will be designed accordingly in order to validate the concept of the smart gate driver. This prototype must include a switching cell made of wide band gap device, e.g SiC MOSFET, and the associated gate driver. The performance of the system will be evaluated experimentally, mostly using double pulse operation.

Detailed objectives / organization

The internship will take place at MERCE, located in Rennes, and will entail the following tasks:

- Review of the state-of-the-art of smart gate driver for dead-time reduction
- Development/simulation of gate driver circuit based on the MERCE's concept
- Proposition of a design procedure
- Design of the prototype for experimental evaluation according to the design procedure
- Experimental validation of the designed set-up

Prerequisites

- Engineer/Master level student with interest in research;
- Strong interest in Power Electronic and Analogic Electronic;
- Understanding of hardware implementation of power electronic set-up;
- Knowledge in LTspice and Altium Designer are an asset;
- Strong interest in experimentation, and familiar with electrical engineering lab equipment (power supplies, measurement devices, scopes and probes, etc);
- Autonomous, but team player;
- English: spoken / written.

Duration: 6 months

Period: from Feb/March 2023 (possibility of flexibility, depending on schools' internships periods)

Contact: Magali BRANCHEREAU (jobs@fr.merce.mee.com) + Johan LE LESLE (j.lelesle@fr.merce.mee.com)

Thank you to provide us an application letter and your CV mentioning the reference of the internship.

The signature of an Internship Agreement with your school is mandatory.