

## Organisational Information

Sign up at: [www.ecpe.org/events](http://www.ecpe.org/events)

### Registration Deadline:

15 June 2023

### Participation Fee:

€ 855,- \* for industry  
€ 675,- \* for universities/institutes

\* plus VAT

- The regular participation fee includes dinner, lunches, coffee/soft drinks and handouts.
- Upon receipt of registration confirmation via email you are signed-up for the event. The invoice will be sent via email.
- 25 % discount for participants from ECPE member companies.
- 10% discount on university/institute fee for participants from ECPE competence centres.
- Further information (hotel list and maps) will be provided after registration and can be found on the ECPE web page.
- Cancellation policy: Full amount will be refunded in case of cancellation up to 2 week prior to the event. After this date 50 % of the fee is non-refundable (substitutes are accepted anytime).
- The number of participants is limited to 12 attendees.

## Organisational Information

**Organiser** ECPE e.V.  
90443 Nuremberg, Germany  
[www.ecpe.org](http://www.ecpe.org)

**Chairman** Prof. Eckart Hoene  
Fraunhofer IZM

**Organisation** Lena Somschor, ECPE e.V.  
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**Venue** Fraunhofer IZM  
Gustav-Meyer-Allee 25  
13355 Berlin  
[www.izm.fraunhofer.de/en](http://www.izm.fraunhofer.de/en)



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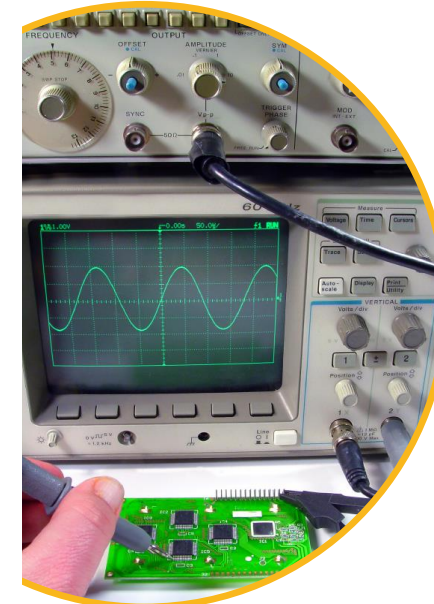
European Center for  
Power Electronics e.V.

## ECPE Lab Course

### EMC Optimised Design (Parasitics in Power Electronics)

22 - 23 June 2023

Fraunhofer IZM  
Berlin  
Germany



## ECPE Lab Course

### EMC Optimised Design

22 - 23 June 2023  
Berlin, Germany

When designing power electronic circuits often electromagnetic properties of layout and construction prevent a proper function. The Know- How for creating working circuits is up to now not well described in textbooks and has to be learned individually by all engineers starting with power electronics. Normally this is accompanied with costly design iterations and many prototypes that slowly lead to an increase in experience.

This lab course is intended to give an insight into the underlying effects by directly carrying out experiments. By investigating the function of a badly designed circuit in the lab a feeling for common mistakes and measurement methods to point them out is given. There is the possibility to modify the circuits and to improve their performance directly.

Different examples for good solutions are shown and finally every attendant has the chance to develop an own design that will be checked by the course instructors for electromagnetic quality. Examples from daily business are also welcome.

#### Course Instructor:

Prof. Eckart Hoene, Fraunhofer IZM

All presentations and discussions will be in English.

## Programme

Thursday, 22 June 2023

09:30 Registration opens

10:00 **Welcome, Introduction**  
Eckart Hoene, Fraunhofer IZM

### Short Coffee Break during 1<sup>st</sup> Lab Session

11:00 **1<sup>st</sup> Lab Session**

A circuit board of an inverter working with 40V and 15A is provided as test object. A check of function will be carried out by the attendees using typical laboratory equipment. Goal is to find out all design mistakes and if possible to find work arounds.

12:30 **Lunch**

13:30 **2<sup>nd</sup> Lab Session**

The work of the first session will be continued. Electrical components and soldering materials are offered for modification of the circuit board.

15:00 **Coffee Break**

16:00 **Discussion of the first results**

The identified mistakes are gathered and possible counter measures discussed. An explanation of the observed effects is given.

16:30 **End of 1<sup>st</sup> Day**

19:00 **Dinner**

## Programme

Friday, 23 June 2023

09:00 **Start of 2<sup>nd</sup> Day**

09:00 **3<sup>rd</sup> Lab Session**

The functionally optimised Circuit Board will be additionally measured for conducted emissions. Dependencies between conducted emissions and the bad layout will be carried out.

10:40 **Coffee Break**

11:00 **4<sup>th</sup> Review of Lab Sessions**

Review & common analysis of failures on the Circuit Board.

12:00 **Lunch**

**5<sup>th</sup> Part  
Presentations**

13:00 **Design Strategies on Board Level**  
Eckart Hoene

13:45 **Parasitic Effects: Design of Commutation Cells and Filters**  
Eckart Hoene

14:45 **Power Module Design for Lower Emissions**  
Eckart Hoene

15:30 **End of Lab Course**