Organisational information

For registration please use the registration form which is available on the ECPE web page: www.ecpe.org
> ECPE Events > ECPE Tutorial: Function and Design of Multilevel and Multicell Converters > Registration Form

www.ecpe.org/ecpe-events

Deadline for registration:

- **3 October 2018**

Participation fee:

- **€ 550,–** * for industry
- € **435,–** * for universities/institutes
- **€ 150,–** * for students/PhD students
  (copy of student ID requested)
  (limited number only)
  (optional dinner: € 50,-* extra fee)

  * plus 20 % French VAT

- The participation fee includes dinner, lunch, coffee/soft drinks and handouts. Students/PhD students can book the dinner for an extra fee of € 50,-*.
- With the confirmation of registration by email you are registered for the tutorial and the invoice will be sent by post.
- 25 % discount for each participant from ECPE Member Companies.
- Further information (hotel list and maps) will be provided after registration and is available on the ECPE web page.
- In case of cancellation later than two weeks before beginning or non-attendance 50 % of the participation fee is payable.
- The number of participants is limited to 35 attendees.

24-Jul-18

Organisational information

Organiser	ECPE e.V. 90443 Nuremberg, Germany www.ecpe.org
Course instructors	Prof. Dr. Marc Hiller Karlsruhe Institute of Technology (KIT) Prof. Dr. Thierry Meynard University Toulouse
Organisation	Lena Somschor, ECPE e.V. +49 (0)911 / 81 02 88 – 18 lena.somschor@ecpe.org
Venue	University Toulouse Laboratoire Laplace Salle du Conseil (F501) 2, rue Camichel 31071 Toulouse, Cedex 7 France

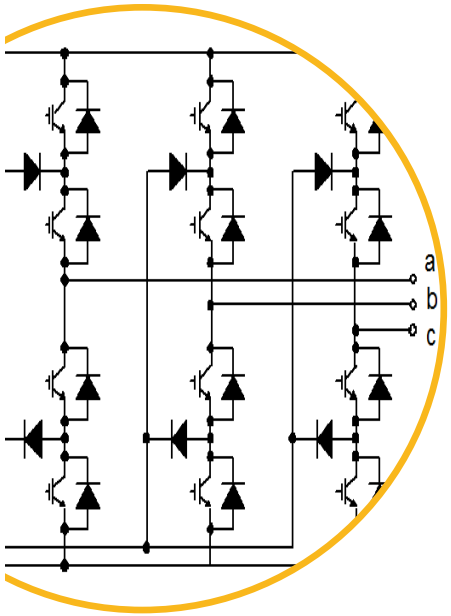
Further information (hotel list and maps) will be provided after registration.

ECPE
European Center for
Power Electronics e.V.

Draft Programme

ECPE Tutorial

Function and Design of Multilevel and Multicell Converters



10 - 11 October 2018
University Toulouse
France

ECPE Tutorial

Function and Design of Multilevel and Multicell Converters

10 - 11 October 2018
Toulouse, France

Compared to the most commonly used 2-Level converters, multilevel converters feature several voltage steps at the output. This allows using power semiconductors which do not have to be rated for the full DC link voltage and avoids series connection of switches. Furthermore this enables higher system voltages for AC and DC applications as well as improved efficiency and reduced harmonic distortion at higher resulting switching frequencies.

In recent years, many 3- and 5-Level converter topologies have been introduced for demanding applications like photovoltaic systems, wind converters, uninterruptible power supplies, MV drives and active filters. In addition, split DC link topologies - like the MMC - are commonly used in power grids (HVDC, SVC) and MV applications.

All of these applications benefit from one or more of the most important advantages of multilevel converters:

+ Improved EMI behavior, less harmonics,
+ Improved efficiency,
+ Use of cost-efficient power semiconductors at lower voltage ratings,
+ Reduction of passive filters (improved power density),
+ Improved availability using redundant components,
+ Higher bandwidth.

Despite these benefits multilevel converters still suffer from some drawbacks:

– Higher parts count and higher design complexity,
– Higher costs, which are only partly compensated by the system benefits,
– Increased control effort.

The training conveys important competencies allowing the professional design, rating and implementation of multilevel/multicell converter based systems.

Who should attend?
The tutorial is designed for R&D engineers, system designers, project managers and (PhD) students interested in power electronic converters and systems, especially for grid and drive applications.

Programme

Wednesday, 10 October 2018

8:45 Registration

9:10 Welcome
Thomas Harder, ECPE e.V.

9:20 **Topologies for Multilevel Converters**
- Overview
- General derivation of topologies

Thierry Meynard

10:30 Coffee Break

10:50 **Power Semiconductors for Multilevel Converters**
- Requirements
- Selection
- Materials (Si/SiC)

Marc Hiller

12:10 Lunch

13:00 **3L-NPC Basics I**
- Circuits, switching states and commutations
- Modulation, voltage balancing
- Losses and loss distribution
- Short-circuit treatment

Thierry Meynard

14:20 **3L-NPC Basics II**
- Designs with IGBTs/IGCTs
- Filter design and passive components
- Interaction with the electrical machine

Marc Hiller

15:30 Coffee Break

15:50 **Further 3L-Topologies:**
- 3L-ANPC, 3L-TNPC
- Comparison
- LV & MV-applications

Thierry Meynard / Marc Hiller

17:00 **Wrap-up and Discussion**

17:30 **End of 1st day**

19:30 Dinner

All presentations and discussions will be in English language.

Programme

Thursday, 11 October 2018

8:45 **Modular Multilevel Converter (MMC)**
- Properties, modulation, clamping behaviour
- Types of submodules
- Applications

Marc Hiller

10:15 Coffee Break

10:30 **Cascaded H-Bridge Converter**
- Properties, modulation, output behaviour
- redundancy, application examples

Thierry Meynard / Marc Hiller

11:45 **Flying Capacitor Topologies**
- Circuit Topologies
- Switching states, commutations, modulation
- Application examples

Thierry Meynard

13:00 Lunch

14:00 **Stacked Multicell Converter**
- Topologies, switching states, commutations
- Modulation, voltage balancing
- Application examples

Thierry Meynard / Marc Hiller

15:30 **Conclusion and discussion**
Thierry Meynard / Marc Hiller

16:00 End of Tutorial

In order to give a system-oriented design overview the following topics will be covered:

- Overview on multilevel/multicell topologies
- 3- and 5-Level converters,
- Modular multilevel converters (MMC)
- Design aspects and features of multilevel converters:
  - Semiconductor losses and modulation
  - Voltage balancing, fault management, redundancy, filter design
- Application examples

Speakers:
Prof. Dr. Marc Hiller
Karlsruhe Institute of Technology (KIT)

Prof. Dr. Thierry Meynard
University Toulouse - Institute LAPLACE