ENIAC-PAB-164-13

Communication to the Governing Board of the ENIAC Joint Undertaking regarding the selection of project proposals and the allocation of public funding following negotiations for Call 2012-2

EXCERPT

ANNEX 2

Acronym	**AGATE**
Duration of project	**36 months**
Date of end of negotiation	**6/12/2012**
Project start date	**1/1/2013**

PROJECT SUMMARY

Development of Advanced GaN substrates & Technologies

Objectives

According to the High-Level Experts Group (HLG) micro and nanoelectronics are essential for all goods and services which need intelligent control in all innovative sectors and are therefore identified as Key Enabling Technologies (KET). Although Silicon-based devices are offering the low-cost high volume capacities and leading edge devices architectures, wide bandgap materials are getting more and more attractive thanks to their high performances for More than Moore applications. For example in switching applications, Si is running out of steam due to its limitations in material properties.

Gallium Nitride is an advanced semiconductor material with high carrier mobility, a platform for many structures, and represents huge potential to enable breakthroughs in various applications like power converters, LEDs, RF or solar cells. The deployment of these technologies is key for Europe to strengthen its competitiveness while addressing societal challenges on transportation, energy efficiency, and renewable energy.

Manufacturing capabilities have been limited by the compatibility of the wafer with silicon production environment: diameter, cost, handling, and material quality. The aim of this KET proposal is to show that innovative GaN-based substrates and devices can be manufactured in a standard process line, with adapted equipment at a cost competitive level on 6 inch wafers, while keeping open the route to 8 inch.

The project aims at covering the whole value chain from material & equipment to device makers with a specific focus on advanced substrates and power devices and the creation of three pilot lines.

The project plans to set-up three pilot lines for GaN-based advanced substrates and devices to help the introduction and market acceptance of these new technologies.

A major goal of the project is to bring a high level of innovation thanks to substrate engineering: the leading edge layer transfer technologies gives access to customized thin film stacking, high performance and Coefficient of Thermal Expansion (CTE) matching. The objective is to implement an advanced pilot line for GaN engineered substrate to create an industrial European source of GaN based on engineered substrates and improved epitaxial structures.

Superior performances such as higher voltage, larger temperature range, but also better reliability and lifetime with respect to the classical GaN on Si epitaxial wafers approach will need to be demonstrated on relevant high power devices such as 600-1200V Schottky Barrier Diodes and High Electron Mobility Transistors. In order to cover all these aspects and thus contribute to map an essential part of the GaN value chain, the different end-user partners propose complementary device pilot lines.

Work and consortium

Soitec will lead the consortium and be the project coordinator.

The consortium is well balanced and covers the full value chain from material to devices: substrates and material suppliers (Soitec, Plansee, Okmetic), equipment suppliers (Aixtron, EVG, Picosun), power device makers (ONSemi and ST), optoelectronics (TopGaN), and solar application (GPTech)

and space application (CRISA). It includes main actors from research institutes (CEA-LETI, CSIC-CNM, Unipress, VTT, Aalto).

Expected results

The expected results are the manufacturing in small volumes of innovative demonstrators on GaN advanced substrates and GaN-based high power switches devices with substantially improved performance. The objective is to deliver these prototypes to the potential customers.

Another outcome expected is to evaluate the good cost structure to penetrate the market: high yield, acceptable substrate wafer cost, low manufacturing and assembly cost.

The proposed European GaN lines shall demonstrate the capability of the equipment and materials for an industrial environment.

Finally, feasibility demonstrations and innovations are expected in optoelectronics or energy application.

Impact

These pilot lines upstream will foster innovation of EU players and support demonstrator projects. Typically key players in automotive or energy conversion are expecting the emergence of GaN substrates and devices availability to develop innovative and competitive systems.

The expected impacts

- Job creation for the material provider and its ecosystem
- Job creation or safeguarding along the value chain
- Investments in the substrate pilot line
- Securing European semiconductor manufacturing capacity and autonomy

This project will generate multiple interactions between material and tool suppliers, substrate manufacturer and end users. All these partners cover a large and continuous part of the European GaN value chain. Thus, the project will lay the foundations of a robust European GaN technology ecosystem enabling long-term and sustainable growth.

Maximum eligible costs and public funding

The negotiation concluded with the following eligible costs (final). The national funding figures are indicative until the establishment of the national grant agreements.

Beneficiary	**Country**	**Eligible cost**	**ENIAC JU Funding**
SOITEC	FR	37,349,867.00 €	5,602,480.00 €
STMicroelectronics (Tours) SAS	FR	709,384.00 €	0.00 €
On Semiconductor Belgium BVBA	BE	7,500,000.00 €	1,125,000.00 €
Green Power Technologies	ES	615,543.00 €	92,331.00 €
PLANSEE	AT	3,678,260.00 €	551,739.00 €
EV Group	AT	946,480.00 €	141,972.00 €
CEA-LETI	FR	8,056,339.00 €	1,208,451.00 €
IHPP PAS	PL	300,000.00 €	45,000.00 €
TOPGAN	PL	250,000.00 €	37,500.00 €
ULPGC-IUMA	ES	233,000.00 €	34,950.00 €
TOTAL		**59,638,873.00 €**	**8,839,423.00 €**

Acronym	**E450EDL**
Duration of project	**36 months**
Date of end of negotiation	**6/12/2012**
Project start date	**1/10/2013**

PROJECT SUMMARY

European 450mm Equipment Demo Line

Objectives

The aim of the E450EDL project is to continue the engagement of the European semiconductor equipment and materials industry in the 450mm wafer size transition that started with the ENIAC JU EEMI450 initiative and proceeded with subsequent projects funded with public money, amongst others NGC450, SOI450, EEM450PR. The demo line resulting from this project will be such that it will enable first critical process module development by combining imec infrastructure with tools remaining at the site of the manufacturers (distributed pilot line). Multi-site processing will allow partners to participate in the world first 450mm integration studies and will be enabled by the controlled exchange of 450mm wafers between different sites.

Work and consortium, expected results

The consortium comprises 43 members from 11 different European countries with many SMEs and research institutes. The project is organized in five technical work packages and a work package on management and coordination.

- In the work package on integration and wafer processing first critical modules will be developed and will demonstrate the feasibility of processing on 450mm wafers.
- The main objective in the work package on lithography is to develop a wafer stage test-rig, which can be implemented into the pilot line system.
- In the work package on front end equipment several tools will be developed such as a plasma ion implant module, a plasma dry etch module, a RTP system and a single wafer cleaning system.
- Furthermore, in the dedicated work package on metrology 450mm metrology tool types will be developed for amongst others dielectric film thickness and composition measurements, defect inspection, defect review and analysis, optical critical dimensions (CD), overlay (mask and wafer) and 3D metrology.
- Finally, from the work package on wafer handling and automation a set of equipment will be provided to support the demo line operations, and facilitate the R&D dedicated to process and metrology modules.

Impact

The European equipment and materials manufacturers have a leading position and sizable market share globally. The transition to 450mm is expected to take place around 2017 under the pressure of the early adopters of new technologies. Traditionally, when such a change happens every about 15 years, the semiconductor industry takes advantage to reconsider options adopted in the previous generation and introduce significant innovation. Engaging early and strongly in preparing the transition to 450mm is one of the strategic priorities of the European industry that will enable Europe to conserve and further develop its leadership position.

Maximum eligible costs and public funding

The negotiation concluded with the following eligible costs (final). The national funding figures are indicative until the establishment of the national grant agreements.

Beneficiary	Country	Eligible cost	ENIAC JU Funding
ASML Netherlands B.V.	NL	50,000,000.00 €	7,500,000.00 €
Adixen Vacuum Products	FR	3,023,809.00 €	453,571.00 €
AIS Automation Dresden GmbH	DE	880,100.00 €	132,015.00 €
Applied Materials Israel Ltd.	IL	29,961,200.00 €	4,494,180.00 €
artemis control AG	CH	543,118.00 €	81,468.00 €
ASM Belgium N.V.	BE	1,661,145.00 €	249,172.00 €
ASYS Automatic Systems GmbH & Co. KG	DE	237,376.00 €	35,606.00 €
CEA-Leti	FR	1,085,285.00 €	162,793.00 €
DEMCON	NL	1,078,246.00 €	161,737.00 €
Entegris Cleaning Process (ECP) S.A.S.	FR	452,274.00 €	67,841.00 €
EV Group GmbH	AT	2,994,140.00 €	449,121.00 €
FEI Czech Republic, s.r.o.	CZ	670,000.00 €	100,500.00 €
FEI Electron Optics B.V.	NL	4,604,000.00 €	690,600.00 €
Fries Research & Technology GmbH	DE	420,000.00 €	63,000.00 €
IBS ion beam services	FR	5,098,481.00 €	764,772.00 €
IDE integrated Dynamics Engineering GmbH	DE	1,100,000.00 €	165,000.00 €
imec Interuniversitair Micro-Electronica Centrum vzw	BE	39,880,512.00 €	5,982,077.00 €
Intel Performance Learning Solutions Ltd	IE	2,920,000.00 €	438,000.00 €
Institute of Scientific Instruments of the ASCR, v.v.i.	CZ	100,000.00 €	15,000.00 €
Jordan Valley Semiconductors LTD	IL	4,729,638.00 €	709,446.00 €
KLA Tencor Corporation Israel Ltd.	IL	4,730,128.00 €	709,519.00 €
LAM Research AG	AT	5,405,760.00 €	810,864.00 €
Levitech B.V.	NL	1,632,000.00 €	244,800.00 €
M+W Products GmbH	DE	400,000.00 €	60,000.00 €
Metryx Ltd	UK	1,912,292.00 €	286,844.00 €
MFA Research Centre for Natural Sciences - Institute for Technical Physics and Materials Science	HU	395,000.00 €	59,250.00 €
Mogema B.V.	NL	2,700,000.00 €	405,000.00 €
Nanoplas	FR	3,730,044.00 €	559,507.00 €
Nova Measuring Instruments Ltd	IL	4,360,000.00 €	654,000.00 €
Prodrive B.V.	NL	4,041,250.00 €	606,188.00 €
Recif Technologies S.A.S.	FR	953,054.00 €	142,958.00 €
Reden	NL	900,000.00 €	135,000.00 €
Riber	FR	886,806.00 €	133,021.00 €
Semilab Semiconductor Physics Laboratory Co. Ltd.	HU	864,500.00 €	129,675.00 €
Semilev GmbH	DE	155,000.00 €	23,250.00 €
Soitec S.A.	FR	878,500.00 €	131,775.00 €
SUSS Microtec AG	DE	11,708,000.00 €	1,756,200.00 €
TNO - Nederlandse Organisatie voor Toegepast Natuurwetenschappelijk Onderzoek	NL	4,374,691.00 €	656,204.00 €
Delft University of Technology	NL	1,167,700.00 €	175,155.00 €
VDL Enabling Technologies Group Eindhoven B.V.	NL	2,500,000.00 €	375,000.00 €
Xycarb Ceramics B.V.	NL	338,511.00 €	50,777.00 €
Zeiss SMT GmbH	DE	250,000.00 €	37,500.00 €
TOTAL		**205,722,560.00 €**	**30,858,386.00 €**

Acronym	**EPPL**
Duration of project	**36 months**
Date of end of negotiation	**6/12/2012**
Project start date	**1/4/2013**

PROJECT SUMMARY

Enhanced Power Pilot Line

Objectives

A sustainable and competitive European power semiconductor industry is essential to support the megatrend developments formulated in the Europe 2020 strategy - climate change, energy security, food security, and health & aging population. It is therefore of paramount importance to defend and further extend Europe's leading position in both power semiconductor manufacturing science(s) and the corresponding application domains. Maintaining these core competencies clearly requires a major, comprehensive and carefully coordinated pan-European innovation effort.

EPPL will combine Research, Development and Innovation (R&D&I) to demonstrate market readiness by industrial implementation at an early stage. Second generation power semiconductor devices fabricated in European leading 300mm pilot lines are at the heart of the project, for which manufacturing excellence, cost competitiveness and challenging applications are critical boundary conditions. With this, to leverage the technical characteristics of power devices and foster the trend towards system-in-package integration, advances in packaging technologies become of utmost importance. These aspects will be fully supported by this projects right from the beginning as well.

Work and consortium

Work to be performed includes developing next generation power semiconductors based on 300mm wafers, setting up the required technologies as pilot line manufacturing, and demonstrating the thus achieved reliable and advantageous solutions for a wide range of ENIAC grand challenge application fields.

Based on a common technology base to be developed, the project aims at achieving the realization of demonstrators in a pilot line, and demonstrating production readiness in the large-scale production environments of strategically selected products and technologies. The demonstrators will be verified in fully functional, energy efficient power applications. Thus, this project will establish the technological base for providing leading energy efficient applications enabled by innovations in power technologies.

To enable this, the project will deal with challenges related to process and production technologies, as well as advanced power metallization technologies and dedicated manufacturing processes for thin 300mm wafers:

- Research on next generation of advanced power semiconductor technologies fabricated on 300mm wafers
- Identify and optimize relevant power semiconductor characteristics taking into account demonstrator application requirements of strategic importance
- Setting up a pilot line for next generation power semiconductor production on 300 mm wafers combining at least two European production sites
- Prove reliability and initial yield targets of the power semiconductor pilot line
- Achieve best-in-class productivity in manufacturing leading-edge power semiconductors for advanced, energy efficient industrial, medical and mobility applications
- Optimize chip-to-package interfacing stack for advanced 3D integration capabilities including a 3D pilot line setup for Si interposer
- Strengthen European intellectual property in semiconductor technology, manufacturing and assembly

Global responsibilities will thus be shared in a pilot line stretching across several European countries. To achieve this goal, the project focuses on significant progress to:

- Enhance the core competencies of European companies in the technology development for power semiconductors as well as the ability for production at competitive cost in Europe, thus also supporting the EU Key Enabling Technology (KET) initiative.
- Set up collaborative value chain(s) by early involvement of manufacturing science in academia, semiconductor manufacturers and leading European power electronics application providers.
- Bring semiconductor factories close to leading customers best serving European industry.
- Use User-centred design/development (UCD) approaches defining the products according to application needs providing the optimized technological innovation.

Expected results

The central goal is to extend the leading position of power semiconductors "Made in Europe". The expected improvement addresses technical challenges as well as commercial competitiveness, both in technology research, semiconductor manufacturing, chip/package interconnection technologies and energy efficient applications. Enabling this, a range of unique manufacturing processes and technologies are expected, as are a multitude of product innovations of direct impact onto everyday high-tech life, e.g. eco-friendly generation of solar power, extended ranges in automotive mobility, lower power consumption in illumination or smarter and more powerful medical-diagnostic appliances

Impact

In its Europe 2020 initiative, the European Commission has set ambitious targets for reduction of greenhouse gas emissions, energy efficiency and electro-mobility. Striving towards these goals, power semiconductors designed and manufactured at competitive cost and in sufficient quantities in Europe - enabled by equipment and materials supplied by European companies - will be key enablers. EPPL will not only contribute significantly to this, providing an enhanced pan-European pilot line and securing highly skilled jobs, but also initiate R&D activities that will further boost the IP in the related fields of high-tech knowledge. The leading position of European industry as system provider will be further strengthened by research on advanced packaging technologies for system integration.

Maximum eligible costs and public funding

The negotiation concluded with the following eligible costs (final). The national funding figures are indicative until the establishment of the national grant agreements.

Beneficiary	**Country**	**Eligible cost**	**ENIAC JU Funding**
Infineon Technologies Austria AG	AT	20,125,198.00 €	3,018,780.00 €
CTR Carinthian Tech Research AG	AT	1,373,544.00 €	206,032.00 €
Technische Universität Graz	AT	429,760.00 €	64,464.00 €
Montanuniversität Leoben	AT	486,846.00 €	73,027.00 €
CEST Kompetenzzentrum fur elektro-chemische Oberflachentechnologie GmbH	AT	498,572.00 €	74,786.00 €
Fronius International GmbH	AT	3,955,906.00 €	593,386.00 €
ams AG	AT	10,921,000.00 €	1,638,150.00 €
Plansee SE	AT	793,863.00 €	119,079.00 €
KAI	AT	412,580.00 €	61,887.00 €
EV Group E. Thallner GmbH.	AT	395,440.00 €	59,316.00 €
Infineon Technologies AG	DE	6,031,808.00 €	904,771.00 €
Infineon Technologies Dresden GmbH	DE	5,438,300.00 €	815,745.00 €
Fraunhofer E.V, IISB	DE	2,107,000.00 €	316,050.00 €
Nmb-Minebea GmbH	DE	2,873,500.00 €	431,025.00 €
Philips Healthcare (PHCD)	DE	4,034,500.00 €	605,175.00 €
Technische Universität Dresden	DE	968,546.00 €	145,282.00 €

Fachhochschule Stralsund	DE	610,000.00 €	91,500.00 €
Max-Planck-Institut für Eisenforschung	DE	533,059.00 €	79,959.00 €
Lear	DE	999,300.00 €	149,895.00 €
Philips Healthcare (PHC)	NL	1,419,038.00 €	212,856.00 €
Technische Universiteit Eindhoven	NL	997,230.00 €	149,585.00 €
Heliox BV	NL	442,272.00 €	66,341.00 €
E-MOSS	NL	386,662.00 €	57,999.00 €
Infineon Technologies Italy	IT	2,643,021.00 €	396,453.00 €
Commissariat a l Energie Atomique et aux Energies Alternatives	FR	1,257,643.00 €	188,646.00 €
Presto Engineering	FR	528,396.00 €	79,259.00 €
Adixen Vacuum Products	FR	820,575.00 €	123,086.00 €
Air Liquide electronics Systems	FR	836,552.00 €	125,483.00 €
Entegris Cleaning Process	FR	597,686.00 €	89,653.00 €
SPTS Technologies SAS	FR	715,227.00 €	107,284.00 €
International Iberian Nanotechnology Laboratory	PT	583,200.00 €	87,480.00 €
NANIUM S.A	PT	602,304.00 €	90,346.00 €
TOTAL		**74,818,528.00 €**	**11,222,780.00 €**

Acronym	**Lab4MEMS**
Duration of project	**30 months**
Date of end of negotiation	**6/12/2012**
Project start date	**1/1/2013**

PROJECT SUMMARY

LAB FAB for smart sensors and actuators MEMS

Objectives

According to the outcomes of the High Level Group on KET, the main driving force behind the development of future innovative goods and services will be Key Enabling Technologies (KETs), such as nanotechnology and nanoelectronics including semiconductors. Mastering these technologies leads to play an important role in the R&D, innovation and cluster strategies of many industries are regarded as crucial for ensuring the competitiveness of European industries in today's knowledge economy. During the last decade, "More than Moore" technologies have marked the largest innovation of semiconductor industry by unleashing the major killer apps of today's consumer, health care and industrial market (e.g. MEMS motion sensors, portable healthcare devices and robotics) In this frame, Europe has got some well recognized leading centres of excellence on "More Than Moore" technology and reached the necessary industrial critical mass and investment scale to successfully pursue the development of innovative microelectromechanical systems (MEMS) sensors and 3D packaging

Lab4MEMS aims to establish a European Pilot Line for innovative technologies on advanced piezoelectric and magnetic materials, including advanced Packaging technologies to meet the ever evolving market needs.

Work and consortium

Lab4MEMS is targeting the market drivers in consumer and healthcare application such as body area sensors and remote monitoring. Coordinated technology capabilities are expected generate innovation and fuel the next generation's smart sensors and actuators based on MEMS:

- Micro-actuators, micro-pumps, sensors and energy scavengers, integrated on silicon-based piezoelectric materials (PZT)
- for use in Data Storage, Ink Jet, Health Care, Automotive and Energy Scavenging
- Magnetic field sensors integrated on silicon-based Anisotropic Magneto Resistance (AMR) materials.
- for use in consumer applications such as GPS positioning and mobile phones
- Advanced packaging technologies and vertical interconnections (flip chip, Through Silicon Vias or Through Mold Vias) for full 3D integration.

Lab4MEMs will integrate the whole MEMS manufacturing chain, down to the new packaging processes, to show the viability for future "More than Moore" products and thus, open up new market opportunities for European industry.

The Pilot Line is promoted to reinforce the manufacturing facilities currently located in each respective participating country, aiming to implement and optimize the industrial processes and to validate the supply chains and the demonstrators suitable to penetrate the market. The locations are therefore distributed among the national clusters of the consortia, streaming the operations from front-end to back-end. They are:

1. Agrate (Italy): MEMS Manufacturing, Application labs, advanced material for smart sensors.
2. Kirkop (Malta): MEMS Packaging and Test.
3. Helsinki MEMS Cluster (Finland): wafer for MEMS (i.e. TSV-wafers or C-SOI), pre-processing and equipment for Atomic Layer Deposition (ALD).
4. Grenoble MINATEC (France): PZT's process transfer to ST, MEMS process optimization and failure analysis.

5. Oslo, Microsystems and Nanotechnology – MiNaLab (Norway): MEMS fabrication, new materials and piezo MEMS application.
6. Leuven, the semiconductors cluster (Belgium): optical inspection, analysis and MEMS metrology at die/wafer level.
7. The Netherlands: tools for material deposition and process, RF-MEMS capacitor's application.
8. Radfeld (Austria): Equipments for high-precision Assembly, Bonding and Packaging.
9. Eastern Europe's research clusters of Warsaw (Poland) and Bucharest (Romania): surface analysis and new material's benchmarking, nanotech structures, MEMS device characterization and modelling.

Expected results

The worldwide competition and investment on new Microelectromechanical systems (MEMS) based on piezoelectric and magnetic materials is very tough, especially in Asia (Japan, Korea and also China) and the United States. The industrial priority focuses on both the application and effective manufacturing of commercial products. In fact, despite the presence of research centres at the forefront of advanced material research, in Europe there is still little industrial investment ready to push through.

Lab4MEMS aims at introducing new classes of (non-CMOS) materials into the pilot line for innovative MEMS production, i.e. this project will leverage on piezoelectric PZT thin-film and materials featuring Anisotropic Magneto Resistance (AMR) such as permalloy. Such materials will enable a variety of new key functionalities for next generation MEMS devices.

In addition, the size and cost of the package are increasingly important and the need for advanced packaging solutions will play a crucial role for the next generation of Smart Sensors. Even if there are several research centres across Europe studying the System in Package approach or full 3D package integration, this technology has been primarily adopted for memory devices. Lab4MEMs is therefore aiming at developing specific 3D package integration for MEMS products. In terms of packaging, the MEMS sensor has to face specific issues since it is not a simple static die but a moving machinery and/or sensing structure with particular constraints due to its function. The approach of Lab4MEMs will integrate the ASIC die & the MEMS sensors in a System in Package 3D configuration, thus enhancing the functionality and reliability while reducing the overall package size and cost, through exploitation of alternative interconnection technologies to the standard wire bonding process, e.g.: flip chip, Through Silicon Vias or Through Mold Vias.

Impact

Microelectromechanical systems (MEMS) have become a key enabling technology for many of today's high-technology products. Actually, it is the promise of MEMS supporting new breakthroughs in areas such as green energy, automotive and radical medical innovations that makes the MEMS industry a key for the fate of European advanced manufacturing as well as for the jobs, innovations and numerous applications (including security and defence) that MEMS have already enabled.

The main manufacturing site of the Lab4MEMS Pilot Line will be based Agrate Brianza (Italy) on 200 mm wafer scale (with a forward looking impact analysis for a future move to 300mm wafer) and it will process more than 600 wafers/week, once in operation. A new set of R&D equipment and tools for PZT and AMR will be placed on top of a larger manufacturing facility already in place in Agrate Brianza for high volume production of 3-axis MEMS accelerometers and gyroscope (i.e. >100M devices/month). This strategy will allow to leverage and increase the know-how on those very strategic enabling technologies, combining scientific skills with the ability to design and manufacture a wide range of smart micro-nano systems on silicon.

The Packaging Pilot line will be based at ST Malta (Kirkop). A site with a vast experience of back-end technologies and a production of 3 million MEMS devices per day (Motion sensors, Microphones and Pressure Sensors)

Last but not least, European SME's and other fabless companies across Europe will benefit from this pilot line offering them a manufacturing route for their innovative future products. Such a manufacturing pilot line is not available in Europe today and also access to these technologies outside Europe is often impossible for those SMEs.

Maximum eligible costs and public funding

The negotiation concluded with the following eligible costs (final). The national funding figures are indicative until the establishment of the national grant agreements.

Beneficiary	**Country**	**Eligible cost**	**ENIAC JU Funding**
STMicroelectronics srl (Coordinator)	IT	5,575,600.00 €	836,340.00 €
ST-POLITO s.c.a.r.l.	IT	283,010.00 €	42,452.00 €
Politecnico di Torino	IT	527,000.00 €	79,050.00 €
Istituto Italiano di Tecnologia	IT	374,750.00 €	56,213.00 €
Politecnico di Milano	IT	470,000.00 €	70,500.00 €
Consorzio Nazionale Interuniversitario per la Nanoelettronica	IT	1,349,500.00 €	202,425.00 €
Commissariat Energie Atomique Et Aux Energies Alternatives	FR	992,876.00 €	148,931.00 €
SERMA Technologies SA	FR	1,213,684.00 €	182,053.00 €
STMicroelectronics Ltd.	MT	4,285,714.00 €	642,857.00 €
University of Malta	MT	294,118.00 €	44,118.00 €
SolMateS BV	NL	463,750.00 €	69,563.00 €
Cavendish KINETICS BV	NL	1,139,200.00 €	170,880.00 €
Okmetic OY	FI	1,506,542.00 €	225,981.00 €
VTT Technical Research Centre of Finland	FI	1,363,153.00 €	204,473.00 €
PICOSUN OY	FI	918,900.00 €	137,835.00 €
KLA-Tencor	BE	2,343,600.00 €	351,540.00 €
University POLITEHNICA of Bucharest	RO	529,412.00 €	79,412.00 €
Instytut Technologii Elektronowej, Warsaw	PL	732,000.00 €	109,800.00 €
Stiftelsen SINTEF	NO	1,668,001.00 €	250,200.00 €
Sonitor Technologies AS	NO	474,930.00 €	71,240.00 €
Datacon Technology GmbH	AT	1,990,665.00 €	298,600.00 €
TOTAL		**28,496,405.00 €**	**4,274,463.00 €**

Acronym	**Places2Be**
Duration of project	**37 months**
Date of end of negotiation	**6/12/2012**
Project start date	**3/12/2012**

PROJECT SUMMARY

Pilot Lines for Advanced CMOS Enhanced by SOI in 2x nodes Built in Europe

Objectives

Traditional planar bulk CMOS transistor architecture at present leading edge of miniaturization is plagued by limitations due to unacceptably high current leakages and variability. To cope with these intrinsic limitations there is a need to speed up the deployment and volume manufacturing of innovative CMOS 2X nm technologies with the advantage of Fully Depleted (FD) undoped channel devices. At the moment, there are two main transistor architectures which can apply to offer Fully Depleted undopped channel devices. The first candidate architecture is the 3D FINFET which uses on gate surrounding the fully depleted channel; the second one is the 2D FD Silicon on Insulator (FDSOI) transistor.

The FD Silicon on Insulator (FDSOI) transistor architecture offers a distinct advantage, especially for the Ultra Low Power applications. FDSOI is enabling a high range Forward and Reverse Body Bias (FBB/RBB) which allows dynamically adjusting the High Performance / Low Power trade-off of a running circuit or portion of circuit. This unique possibility allows switching from Low Power (LP) to High Performance (HP) modes only when requested and to minimize the overall power consumption which is now the blocking factor for the continuous integration of new functions in the future convergence circuits. PLACES2BE is entirely devoted to the FDSOI.

The general goal of this project is the industrialization of 28/20nm Fully Depleted (FD) Silicon On Insulator (SOI) Technology platforms, enabling 2 different sources in 2 different European countries. The project also aims at establishing and reinforcing a design ecosystem in Europe using these platforms. Last, the project considers extremely important to explore extension towards FD devices at 14/10nm, in order to continue the road toward more efficient technologies.

Work and consortium

PLACES2BE aims at introducing the FDSOI technology for the first time in mainstream digital CMOS for consumer applications, in the Internet multimedia communication field and other applications requiring highly energy efficient digital electronics, such as mixed signal applications addressing the whole range of future societal needs such as safety, health and well-being, energy. PLACES2BE will also exploit the capabilities of the FDSOI advanced CMOS technologies for RF and AMS designs.

This project will achieve the following breakthroughs:

- First 28 nm and then 20 nm FDSOI capacity installed in the World
- First 20 nm CMOS capacity installed in Europe
- Offer of wide dynamic range with the most energy efficient technologies: able to address both low power and high performance applications
- The 28 nm (respectively 20 nm) FDSOI technology should be able to offer 20% performance (speed) improvement over its bulk counterpart at nominal voltage, a wider voltage range operation around 0.4 to 1.2 V with up to a 10x speed boost at 0.4V, as well as a greatly enhanced energy efficiency from 20% in the high range of operating voltage to a factor of 2.5 (-60%) in the lower range of operating voltage
- Offer the capability to dynamically adjust the devices performance / power tradeoff thanks to the back biasing feature

For achieving success the project will implement a number of activities in parallel, and will be carried by a project consortium expanded to include all necessary competencies and contributions:

- Technology Robustness
    - Necessary evolutions of the technology modules to cope with their integration into industrial processes. This will require working on all specific aspects of planar fully depleted CMOS including substrate advances, module and device evolution, hybrid implementation of bulk and SOI technology, back bias management
    - Defectivity studies, specific to the FDSOI technologies concerning all relevant processes as well as the substrates. Specific test vehicles will be developed to this aim.
    - Yield ramp studies to qualify rapidly the technologies. In terms of efforts this is the largest part of the project due to the very high cost of advanced technologies
- Multiple source enablement
    - The concept of Pilot Line entails a road to industrialization. This project will ensure this by preparing, first within the consortium in its 2 places of operation but bearing in mind possible other partners, the technology transfer. This means completely revising the portability issues, from the start
- Technology Design enablement
    - A technology can only be used in as much as the tools for using it are available and stable. This means ensuring the availability of a set of tools from Design Rule Manual to OPC to high level CAD tools including models both for digital and for RF applications as well as libraries that allow a fast design work. All these elements are embodied in the release of Design Kits
- State of the art demonstrators and prototypes
    - The usability of a technology platform depends on the performance (speed, area, energy efficiency, noise, max frequency, precision…depending on the type of application) of the circuits that it enables. The project includes leading European companies, academic labs as well as smaller companies implementing innovative designs to exercise the technology. The project also plans to open multi project wafer services for select entities, outside the project at project start
- Reliability of technology and design
    - Due to the very small dimensions of all parts of the devices and the variety of materials involved, specific reliability studies will be conducted. This will include physical characterization techniques to study e.g. trapping and degradation mechanism. This will also include not only device wafer level but circuit reliability. Last, the project will study Front-End, Back-End and packaging reliability
- Forward looking studies to prepare the next technology stages
    - The strength of the CMOS technology over several decades has been to offer a series of technology generations, each enabling greater performance than its predecessor, while keeping enough commonalities to take advantage of legacy. It is therefore extremely important to forecast the subsequent stages while developing the current and next ones. This project will thus include forward looking tasks envisioning the next stages “14 and 10 nm”.

Impact

The expected impact of the proposed innovation deployed in PLACES2BE will be

- A strengthening the nanoelectronics manufacturing capabilities in Europe, both in terms of the direct effect in skilled jobs and the indirect impact upon all other contributiong industries, particularly in the SMEs sector, delivering services and equipment to the nanoelectronic devices manufacturers. This project will take advantage of the most advanced materials and processing equipment, a significant portion of it being produced in Europe
- The reinforcement of the European IP and Fabless ecosystem. IP and Fabless companies shall work synergistically with - and benefit from - the developments driven by manufacturing companies (equipment, materials, IDM, Foundry). For Europe, it is essential to master both aspects in order to master the whole value chain

- Early opening to new applications. By gaining experience e.g. with the RF capabilities of FD technologies, European partners will have a heads start to new possibilities in the application domains
- The strengthening of the relationships between industry and academia throughout Europe. This will also have an impact on education, and essential element for the sustainability of the industry in Europe. Additionally, PLACES2BE will contribute to the cluster policy that is an integral part of the Horizon 2020 strategy.

PLACES2BE Pilot line is thus fully in line with the ENIAC Vision and Mission statements and with the associated SRA. It aims at implementing 2 physical PLACES where those innovations can be industrialized, benefiting the whole value chain: from device physics, to equipment assessment, technology development, modelling, CAD tools, design, and applications. PLACES2BE is therefore also a distributed research infrastructure in the nanoCMOS domain. Beyond the direct impact induced by the material and intellectual investment, it will positively impact the whole value chain of digital electronics in Europe.

Maximum eligible costs and public funding

The negotiation concluded with the following eligible costs (final). The national funding figures are indicative until the establishment of the national grant agreements.

Beneficiary	**Country**	**Eligible cost**	**ENIAC JU Funding**
STMicroelectonics SAS Crolles 2	FR	205,368,935.00 €	30,805,340.00 €
STMicroelectronics SA	FR	27,832,925.00 €	4,174,939.00 €
STMicroelectonics SAS Grenoble	FR	14,950,112.00 €	2,242,517.00 €
ST-Ericsson (Grenoble) SAS	FR	9,380,650.00 €	1,407,098.00 €
CEA/LETI	FR	65,665,655.00 €	9,849,848.00 €
SOITEC SA	FR	2,000,000.00 €	0.00 €
Adixen	FR	3,628,124.00 €	544,219.00 €
Mentor Graphics	FR	1,619,642.00 €	242,946.00 €
Ion Beam Services	FR	3,979,640.00 €	596,946.00 €
Institut Polytechnique de Grenoble	FR	945,726.00 €	141,859.00 €
Dolphin	FR	2,141,639.00 €	321,246.00 €
Université Catholique de Louvain	BE	396,000.00 €	0.00 €
IMEC	BE	515,160.00 €	77,274.00 €
ST-Ericsson Oy (Finland)	FI	4,352,050.00 €	652,808.00 €
GlobalFoundries	DE	5,719,000.00 €	0.00 €
Forschungzentrum Jülich	DE	499,382.00 €	74,907.00 €
University of Twente	NL	930,784.00 €	139,618.00 €
Axiom	NL	546,000.00 €	81,900.00 €
Bruco Integrated Circuits	NL	600,000.00 €	90,000.00 €
eSilicon	RO	921,600.00 €	138,240.00 €
ACREO	SE	358,280.00 €	53,742.00 €
ST-Ericsson (Lund)	SE	5,376,900.00 €	806,535.00 €
Ericsson AB	SE	1,110,000.00 €	166,500.00 €
TOTAL		**358,838,204.00 €**	**52,608,482.00 €**