Organisational Information

Sign up at: www.ecpe.org/events

Registration Deadline:

2 October 2022

Participation Fee:

€ 320,– *	for industry
€ 290,– *	for universities/institutes
€ 120,– *	for students/PhD students (limited spaces; copy of students ID required)

* plus VAT

- The participation fee includes lectures and digital proceedings (provided 1 day prior to the event by email)
- Participation by web conference tool (Webex). Access data will be provided by email.
- Upon receipt of registration confirmation via email you are signed-up for the event. The invoice will be sent via email.
- ECPE members are able to register 1 participant free of charge, 25% discount for further participants.
- 10 % discount for participants from ECPE competence centres.
- Further information (hotel list and maps) will be provided after registration and can be found on the ECPE web page.
- Cancellation policy: Full amount will be refunded in case of cancellation up to 1 week prior to the event. After this date and in case of no-show 50 % of the fee is non-refundable (substitutes are accepted anytime).
- The number of participants is limited to 35 attendees.

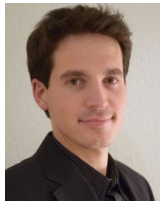
21/07/22

Organisational Information

Organiser	ECPE e.V. 90443 Nuremberg, Germany www.ecpe.org
Organisation	Marietta Di Dio, ECPE e.V. +49 911 81 02 88 – 13 Marietta.didio@ecpe.org

Course Instructors:

Dr. Reinhold Bayerer,
Physics of Power Electronics (D)



Prof. Thomas Basler
Chemnitz University of Technology (D)

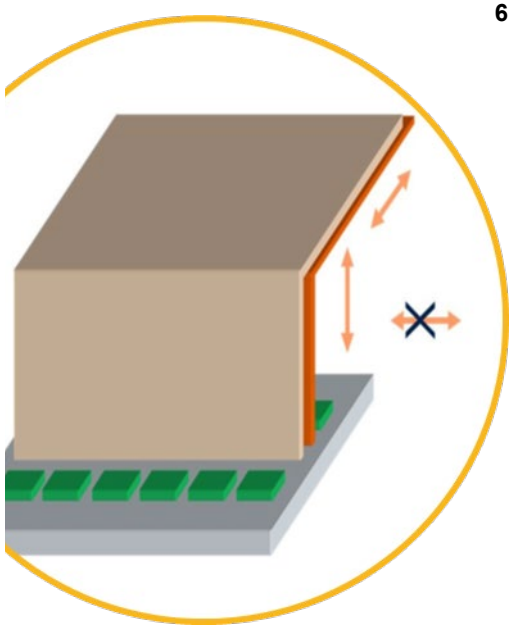
European Center for
Power Electronics e.V.

Digital Event

ECPE Online Tutorial

Power Circuits for Clean Switching and Low Losses

6 – 7 October 2022



ECPE Online Tutorial

Power Circuits for Clean Switching and Low Losses

6 - 7 October 2022
Digital Event

This tutorial will teach the various effects of parasitic inductance (L_S) in power electronics. As power density and current density is continuously rising, parasitic inductance and resistance become more and more the limiting factors. The problem is the product inductance times current (L_S*I) rising, simultaneously, if designs do not improve.
Not only overvoltage during switching is the problem but for bipolar power semiconductors like IGBTs and freewheeling diodes, parasitic inductance causes disadvantageous current waveforms.
In systems which have snubber capacitors additional to the DC-link capacitor and parasitic inductance in between, oscillations between these capacitors occur.
When considering power semiconductors in parallel the current sharing of controlled devices like IGBT, MOSFET and JFET can be affected by the presence of small parasitic inductance.
Parasitic inductance in the control circuit (gate circuit) decouples driver and the gates of the devices leading to increased short circuit current, for example.
To introduce these topics the tutorial will start with the basics of switching inductive loads and discussion of related waveforms. Investigations on the different effects will follow. The discussion of paralleling will be accompanied by case studies. Geometries of conductors and system design for low parasitic inductance and good current sharing will be another main part and the conclusions will summarize the benefits of related system design – clean switching and low losses.

All presentations and discussions will be in English.

Programme

Thursday, 6 October 2022

8:30 *Start of Webex meeting*

9:00 **Welcome and tutorial opening**
ECPE

9:15 **Power Semiconductors Switching Inductive Load and Parasitic Inductance**
Reinhold Bayerer

10:20 Break

10:30 **Geometry of Conductors and their Inductance – Determination and Evaluation**
Reinhold Bayerer

11:45 Lunch break

12:30 **Parasitic Inductance – Effecting Switching Characteristics and Stress Factors of Power Semiconductors**
Reinhold Bayerer

13:05 **Turn-off Behavior of Bipolar Devices – IGBT and Diode: Influence of DC-Voltage, Current and Gate Control**
Thomas Basler

14:00 Break

14:20 **Turn-off Behavior of Bipolar Devices – IGBT and Diode: Influence of DC-Voltage, Current and Gate Control**
Thomas Basler

15:30 Break

15:45 **Parasitic Inductance – Effecting Current Sharing of Paralleled Power Devices**
Reinhold Bayerer

16:45 **Case Study I: Asymmetric Paralleling and Discussion**
Reinhold Bayerer

17:15 End of first day

Programme

Friday, 7 October 2022

8:30 *Start of Webex meeting*

8:45 **Case Study II: Asymmetric Paralleling and Discussion**
Reinhold Bayerer

9:10 **Parasitic Inductance – Effecting System Losses**
Reinhold Bayerer

9:40 Break

9:50 **Oscillations in DC-Bus**
Reinhold Bayerer

10:40 **Parasitic Inductance meets Parasitic Resistance**
Reinhold Bayerer

10:50 Break

11:00 **Gate Inductance**
Reinhold Bayerer

11:40 **Parasitic Capacitance and Aspects of EMI**
Reinhold Bayerer

12:15 Lunch break

13:00 **Clean Switching of WBG Devices – Part I**
Thomas Basler

14:00 **Clean Switching of WBG Devices – Part II**
Thomas Basler

15:00 Break

15:15 **Clean Switching of SiC Devices**
Reinhold Bayerer

16:05 **Measuring Challenges and Solutions**
Reinhold Bayerer

16:20 **Benefit of Circuits with Low Parasitic Inductance**
Reinhold Bayerer

16:45 **Open Questions and Discussion**

17:15 End of Tutorial