Registration (Fax Reply)

To: ECPE e.V.
Att.: Ingrid Bollens, ingrid.bollens@ecpe.org
Please **e-mail** a scanned copy of the completed form or send a fax to: +49 (0)911 / 81 02 88 – 28

Register before **19 January 2012**

Participation fee:
- ❍ **€ 350.–** for industry
- ❍ € **260.–** for universities/institutes
- ❍ **€ 80.–** for students/PhD (shortened workshop package)

The fee includes dinner, lunch, coffee/soft drinks and a CD with the workshop presentations. A printed version of the workshop handout is available on request (€ 42.--).

With the confirmation of registration you will receive the invoice. In case of cancellation after 19 January 2012 or non-attendance 50 % of the participation fee are payable.

Three participants from each ECPE member company free of charge. Allocation in sequence of registration.

Sender:

Title, given name, name

Company, department

Full address

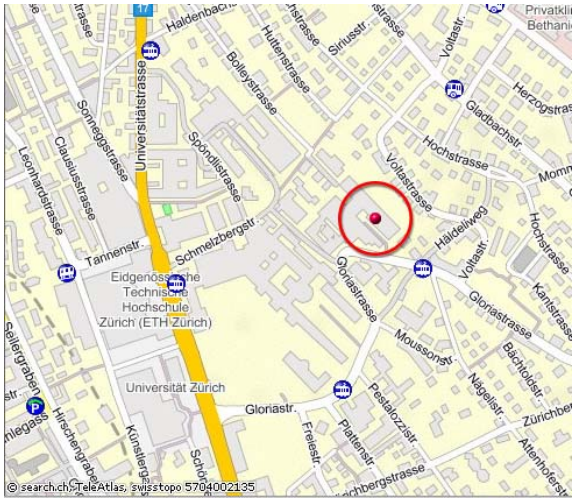
Phone, fax

E-mail

Date, signature

Organisational information

Organiser	ECPE e.V. 90443 Nuremberg, Germany www.ecpe.org
Chairman	Prof. Dr. Johan W. Kolar ETH Zurich Prof. Dr. Dieter Silber, University Bremen Prof. Dr. Leo Lorenz, Infineon Technologies/ECPE e.V.
Organisation	Ingrid Bollens, ECPE e.V. +49 (0)911 / 81 02 88 – 10 ingrid.bollens@ecpe.org
Workshop venue	ETH Zurich (Eidgenössische Technische Hochschule Zürich) Rämistraße 101 Main Building, Room HG F30 8092 Zurich, Switzerland



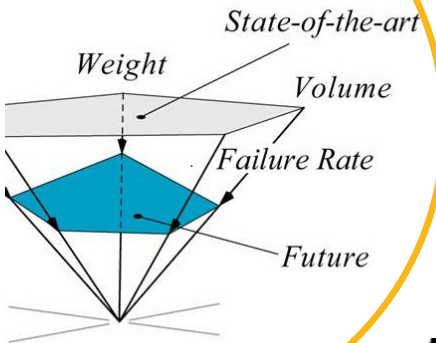
Further information (hotel list and maps) will be provided after registration.

ECPE
European Center for
Power Electronics e.V.

Programme

ECPE Workshop

Future Trends for Power Semiconductors



26 Jan. (evening session) – 27 January 2012
ETH Zurich
Zurich, Switzerland

in cooperation with

ETH
Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Universität Bremen

Future Trends for Power Semiconductors

26 Jan. (evening session) – 27 January 2012
Zurich, Switzerland

Power semiconductors are key components in power electronics systems and along with digital control a significant driver of innovation today. The conduction and switching losses of the components have been continually reduced in the past. Complemented by extraordinary progress in packaging and power module technology, this led to substantial improvements in the power density and efficiency of power electronics converters.

Current developments in the field of wide–bandgap semiconductors again promise significant improvements in switching and conduction behaviour. And from Si based devices further progress is expected as well. Exploitation of this potential, however, requires wide-ranging research activities, both regarding component concepts and also with respect to the possibility of hybrid and (applicable especially to GaN) monolithic power integration. The system concepts must also be re-evaluated. The question of the development of SiC high voltage components as an alternative to the Si multi-level configurations may serve here as an example.

In this situation the decreasing number of university chairs with research emphasis on Power Semiconductors is of special concern. Hence within the framework of this workshop, not only technical aspects should be discussed, but also future university research and teaching, and co-operation with industry.

The workshop is chaired by Prof. Dr. J.W. Kolar (ETH Zurich), Prof. Dr. D. Silber (University Bremen) and Prof. Dr. L. Lorenz (Infineon/ECPE). All presentations and discussions will be in English.

Thursday, 26 January 2012

Venue of Evening Session
ETH Zurich , Main Building, room HG F30
8092 Zurich, Switzerland

17:30	Start of Registration / Welcome reception
17:45	**Welcome Address, Opening** J.W. Kolar, ETH Zurich, L. Lorenz, ECPE e.V.
18:00	**Keynote: Power Semiconductors – A Main Driver of Power Electronics Development** R. W. De Doncker, RWTH Aachen (D)
18:30	**Keynote: Role of Research Institutes and Universities in Power Device Development, from Industrial Point of View** S. Linder, ABB Switzerland (CH)
19:00	**Discussion**
19:30	**Transfer by bus to dinner place Hotel "Zürichberg"**
20:00	Dinner at Hotel "Zurichberg" Orellistrasse 21, 8044 Zurich

Friday, 27 January 2012

Venue: ETH Zurich , Main Building, room HG F30
8092 Zurich, Switzerland

Requirements for the Future

8:15	**Keynote: High Power Density Systems: Requirements on Future Devices and Integration Concepts** D. Boroyevich, VPEC (US),
9:00	**Requirements for Power Semiconductor Devices in Energy Distribution and Transmission Systems** P. Steimer, ABB Switzerland (CH)
9:30	**New High Power Topologies and Impact on Device Requirements** P. Nee, KTH (SE)
10:00	**Parasitics in Power Electronics: Avoid Them or Turn Enemies into Friends** M. Maerz, Fraunhofer IISB (D)
10:30	Coffee Break

Si, SiC, GaN – Part 1

11:00	**Keynote: Si, SiC, GaN - How Will They Share Future Applications?** I. Omura, Kyushu Institute of Technology (JP)
11:45	**Future and Expected Applications of Si Devices** F. Udrea, University of Cambridge (UK)

Friday, 27 January 2012

12:15	Lunch

Si, SiC, GaN – Part 2

13:30	**Future of WBG Devices: What Do We Expect?** J. Millan, Centro National de Microelectronica (ES)
14:00	**SMART Power for Automotive Applications** M. Pfost, Reutlingen University (D)
14:30	Coffee Break

Packaging / Reliability

15:00	**Coupling of Power Semiconductors and Parasitics** J. Popovic-Gerber, J.A. Ferreira, Delft University of Technology (NL)
15:30	**Future Module Concepts: Aspects of Reliability and Cooling** U. Scheuermann, Semikron Elektronik (D)
16:00	**Future Module Concepts: Construction and Internal Parasitics** R. Bayerer, Infineon Technologies (D)
16:30	**Requirements for Future Simulation Tools from Industrial Point of View** F. Pfirsch, Infineon Technologies (D)
17:00	**How Power Device Simulation Tools Should Look Like From a Physical Model Maker´s View** G. Wachutka, TU Munich (D)
17:30	**Final Discussion**
17:45	**End of Workshop**