# **Organisational information**

For registration please use the registration form which is available on the ECPE web page: <a href="www.ecpe.org">www.ecpe.org</a> > ECPE Events > ECPE Workshops: Smart Transformers for Traction and Furture Grid Application > Registration Form

#### www.ecpe.org/ecpe-events

#### **Deadline for registration:**

> 28 January 2016

#### Participation fee:

- > €595,- for industry
- > €445,- for universities/institutes
- > €150,- for students/PhD students

(copy of student ID requested)

(limited number only)

(optional dinner: €50,- extra fee)

- The participation fee includes dinner, lunch, coffee/soft drinks and a CD with the workshop presentations. Students/PhD students can book the dinner for an extra fee of €50,-.
- A printed version of the workshop handout is available on request (€50–).
- With the confirmation of registration by email you are registered for the workshop and the invoice will be sent by post.
- > Three participants from each ECPE member company free of charge. Allocation in sequence of registration.
- Further information (hotel list and maps) will be provided after registration and is available on the ECPE web page.
- In case of cancellation later than two weeks before beginning or non-attendance 50 % of the participation fee is payable.

## **Organisational information**

| Organiser    | ECPE e.V.<br>90443 Nuremberg, Germany<br>www.ecpe.org                            |  |
|--------------|--|--|
| Chairmen     | Prof. J.W. Kolar,<br>ETH Zurich<br>Prof. M. Liserre,<br>CAU Kiel                 |  |
| Organisation | Lena Somschor, ECPE e.V.<br>+49 (0)911 / 81 02 88 – 18<br>lena.somschor@ecpe.org |  |
| Venue        | ETH Zurich<br>Main Building, Room HG F7<br>Raemistrasse 101                      |  |

8092 Zurich, Switzerland





# **Programme**

# **ECPE Workshop**

# Smart Transformers for Traction and Future Grid Application



4 – 5 February 2016 ETH Zurich Zurich, Switzerland

in cooperation with







## **ECPE Workshop**

# **Smart Transformers for Traction and Future Grid Application**

4 – 5 February 2016 Zurich, Switzerland

Solid-State Transformers (SSTs) are featuring bidirectional medium-voltage (MV) to low-voltage (LV) AC/AC, AC/DC or DC/DC conversion and are formed by power electronics interfaces at the input and output side, which are linked through a medium-frequency transformer. Accordingly, SSTs show a higher power density / lower weight than conventional low-frequency transformers and are offering high controllability, which can be utilized for defining the power flow, for output voltage / frequency control, reactive power compensation, active filtering etc.

Therefore, SSTs are already perfectly suited for replacing the bulky low-frequency transformers of locomotives, where a simultaneous improvement of power density and efficiency could be achieved. In a more futuristic scenario SSTs can be seen as key elements of a smart hybrid, i.e. AC and DC electric grid, allowing also MVDC and LVDC connectivity, hence an easier integration of renewable energy sources also through the use of storage systems.

However, the connection to MV, the high overall complexity, and the high realization costs are still main challenges for practical applications of SST technology.

The workshop will address the state-of-the art of SST systems from topology and control perspective but also concerning key component technologies like high-voltage SiC power semiconductors and packages and insulation materials and finally also discuss application scenarios in traction systems and electric grids.

The workshop is chaired by Prof. J.W. Kolar (ETH Zurich) and Prof. M. Liserre (CAU Kiel).

All presentations and discussions will be in English language.

## **Programme**

#### Thursday, 4 February 2016

#### 9:00 Start of Registration / Welcome Coffee

9:30 Welcome, Opening
J. W. Kolar, ETH Zürich, T. Harder, ECPE e.V. (D)

#### Introduction

9:50 Future Grids

M. Weinhold, Siemens (D)

10:30 Transformation of the Electric Grid by Solid State Transformer

A. Huang, NC State University, FREEDM Center (US)

#### **SST Concepts and Challenges**

11:00 Solid-State Transformers – Concepts, Challenges and Opportunities

J.W. Kolar, J.E. Huber, ETH Zürich (CH)

11:30 Smart Transformers: System-Level Challenges M. Liserre, CAU Kiel (D)

12:00 Discussion

#### 12:15 Lunch

#### **Industry Applications of Solid-State Transformers**

13:30 Power Electronics Traction Transformers (PETT),
Potentials and Challenges
S. Alvarez, F. Canales, ABB Switzerland (CH)

**14:00 SST for Traction: Status and Challenges**C. Gerster, Bombardier Transportation (CH)

14:30 SiC based Power Block for High Power and High Frequency Applications
R. Datta, P. Sandvik, GE (USA)

15:00 Discussion

#### 15:15 Coffee break

#### **Architectures and Topologies for Solid-State Transformers**

15:45 Topologies and Optimal Design of Hybrid Distribution Transformers

J. Burkard, ETH Zürich (CH)

16:15 The HEART Approach: Reliability through Energy Routing M. Andresen, L. Costa, CAU Kiel (D)

16:45 Derivation and Comparative Analysis of Multi-Cell Isolated Front End and Isolated Back End SSTs
J. E. Huber, ETH Zürich (CH)

#### Which Application for the Solid-State Transformer?

17:15 Forum Discussion with Speakers

18:15 End of 1st Workshop Day

20:00 Dinner

### **Programme**

#### Friday, 5 February 2016

#### **SST System Level Perspectives**

9:00 Flexible Grids and Storage Systems –
DC-DC Converters as a Key Enabling Technology
R.W. de Doncker. RWTH Aachen (D)

10:00 TBD

P. Bauer, Delft University of Technology (NL)

10:30 Discussion

#### 10:45 Coffee break

#### **Power Semiconductors for SST Realization**

11:15 Potentials and Challenges of Silicon Power
 Semiconductors for Solid State Transformer Applications
 M. Rahimo, F. Canales, ABB Switzerland (CH)

11:45 DC Wind Turbine

P.C. Kjaer, Vestas (DK)

12:15 Discussion

#### 12:30 Lunch

13:45 WBG (SiC) Semiconductors for SST applications – state of the art and trends

P. Friedrichs, U. Jansen, Infineon Technologies (D)

14:15 MV Power Electronics with HV SiC Devices

D. Kranzer, Fraunhofer ISE (D)

#### Multilevel Topologies vs. High Blocking Voltage Devices

14:45 Forum Discussion with Speakers

16:00 End of Workshop