

## Registration (Fax Reply)

To: ECPE e.V.  
Att.: Ingrid Bollens  
Fax: +49 (0)911 / 81 02 88 – 28

Register before **23 September 2009**

### Participation fee:

Adv. PE Pack 30 Sep. 2009	Mech. Syst. 01 Oct. 2009	Both Work- shop Days	
<input type="checkbox"/> 350.00 € *	<input type="checkbox"/> 350.00 € *	<input type="checkbox"/> 590.00 € *	Industry
<input type="checkbox"/> 260.00 € *	<input type="checkbox"/> 260.00 € *	<input type="checkbox"/> 440.00 € *	University
<input type="checkbox"/> 80.00 € *	<input type="checkbox"/> 80.00 € *	<input type="checkbox"/> 140.00 € *	Students

The fee includes dinner, lunch, coffee/soft drinks and a CD with the workshop presentations. A printed version of the workshop handouts is available on request (€42,- \*).

With the confirmation of registration you will receive the invoice (\* plus VAT).

In case of cancellation after 23 September 2009 or non-attendance 50 % of the participation fee is payable.

Three participants from each ECPE member company free of charge. Allocation in sequence of registration.

Sender:

\_\_\_\_\_

title, given name, name

\_\_\_\_\_

company, department

\_\_\_\_\_

full address

\_\_\_\_\_

phone, fax

\_\_\_\_\_

e-mail

\_\_\_\_\_

date, signature

## Organisational information

Organiser: ECPE e.V.  
90443 Nürnberg, Germany  
www.ecpe.org

Chairmen: Prof. Dr. B. Allard, INSA de Lyon  
- SEEDS ISP3D  
Dr. G.-M. Martin, MOVEO/Valeo  
T. Harder, ECPE

Organisation: Ingrid Bollens, ECPE e.V.  
+49 (0)911 / 81 02 88 – 10  
ingrid.bollens@ecpe.org

Place of workshop: Hotel Forest Hill Paris La Villette  
28, avenue Corentin Cariou  
75019 Paris, France



Further information (hotel list and maps) will be provided after your registration.

## Draft Programme



**ECPE European Center for  
Power Electronics e.V.**

## Double Workshop Advanced Power Electronics Packaging 30 September 2009 & Mechatronic System Integration 1 October 2009

**Paris, France**  
in cooperation with



# Draft Programme



ECPE European Center for  
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## Double Workshop Advanced Power Electronics Packaging 30 September 2009

&

## Mechatronic System Integration 1 October 2009

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### Programme

## Advanced Power Electronics Packaging

Wednesday, 30 September 2009  
9.00 – 17.15 h

According to Rao R. Tummala the major functions of electronic packaging cover the signal and power distribution, heat dissipation (cooling) as well as mechanical, chemical and electromagnetic protection. This basic packaging definition holds for power electronics as well but in this field packages have to be designed for higher voltages and currents while the heat removal (thermal management) is the key challenge. In microelectronics packaging the most important figure of merit is the wiring (I/O) density while in power electronics power density is key.

Advanced power electronics packaging developments and trends will be presented and discussed in this 1<sup>st</sup> part of the two-day workshop with focus on the low-power side. For power discretes low-profile chipscale packages will be presented. The challenges and limits of System-on-Chip (SoC) and System-in-Package (SiP) integration will be discussed. On module and board level, 3D packaging approaches enabling the integration of power and control will be presented.

Prof. Dr. B. Allard (INSA de Lyon – SEEDS ISP3D) will chair the workshop together with Thomas Harder (ECPE). All presentations and discussions will be in English.

- 9:00 Start of Registration
- 9:15 **Welcome**  
B. Allard, INSA de Lyon, T. Harder, ECPE
- 9:30 **Introduction: Basic Packaging Functions, Thermal Management and Reliability**  
B. Allard, INSA de Lyon

### Chip and Wafer Level Technologies, Power Discretes

- 10:00 **Chip Level Interconnection: Soldering and Sintering; Bond Wires, Clips and Ribbons**  
E. Milke, W.C. Heraeus
- 10:30 **Wafer Level Technologies: Solderable Metallisations, Power Bumping and Balling**  
W. Reinert, Fraunhofer ISIT

### Programme

- 11:00 Coffee break
- 11:20 **Low Profile Power Packages (BGAs, CSPs)**  
STMicroelectronics (invited)
- System-on-Chip (SoC), System-in-Package (SiP)**
- 11:50 **3D capacitors on silicon : technologies and integrated applications**  
M. Brunet, LAAS Toulouse  
C. O'Mathuna, Tyndall
- 12:30 **SiP: DC/DC Converter in Package**  
NXP Semiconductors (invited)
- 13:00 Lunch
- Module and Board Level Packaging**
- 14:15 **PCB based Integration Technology (Power Sandwich Technology)**  
I. Josifovic, J. Popovic-Gerber, TU Delft
- 14:45 **Power Electronics Packages with Embedded Chips**  
L. Boettcher, Fraunhofer IZM, Berlin
- 15:15 Coffee break
- 15:45 **Power Electronics Packaging Roadmap**  
T. Harder, ECPE
- 16:15 Case Studies, Projections, Wrap up and Discussion
- 17:15 End of workshop
- 19:30 Joint Dinner

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## Programme

### Mechatronic System Integration

Thursday, 1 October 2009  
8.30 – 17.00 h

Key driver for Mechatronic System Integration are the severe space, weight and also cost restrictions in emerging applications e.g. in automotive and aerospace. Classic power electronics in the cabinet designs cannot be transferred but power electronics has to be integrated in the mechanical system to optimise the use of space, to avoid expensive cables and fault-prone connectors and to reduce EMI filter complexity. On the other side, the power electronics components and assemblies are exposed to extreme loads in terms of temperature, temperature cycling and vibration. The thermal design of the overall system is very important in power mechatronics taking into account the requirements on reliability and lifetime

Mechatronic integration means that mechanics, power electronics, sensors and control have to form a single functional unit. Traditional interfaces between electronics and mechanics must be dissolved. However, the great challenge with any approach of mechatronic integration is that it must be effective, not only with respect to system size, but also in terms of system costs, functionality, manufacturability, testability and reliability.

Dr. G.-M. Martin (Valeo) who is heading the Mechatronics activities in the French automotive cluster MOVEO will chair the workshop together with Thomas Harder (ECPE). All presentations and discussions will be in English.

8:30 **Introduction**  
G.-M. Martin, Valeo, T. Harder, ECPE

#### Design Challenges for Power Mechatronics

8:45 **Mechanical and Electrical Co-Design**  
Daniel Marson, Dassault System

9:15 **HPC Solutions for Multi Physics Analysis and Multi-Objective Optimization – Opportunities and Limitations for Mechatronics Applications**  
K. Kayvantash, University of Cranfield

#### Key Technologies for Power Mechatronic Integration

9:45 **3D Integration Technologies using Solder-based Interconnection Technologies**  
M. Mermet-Guyennet, Alstom/PEARL

## Programme

10:15	Coffee break
10:45	<b>PCB-based Integration of Power Electronic Systems for Automotive Electronics</b> T. Hofmann, Continental
11:15	<b>Double-Sided Cooling in Automotive Power Electronics</b> A. Schletz, Fraunhofer IISB
<u>Mechatronic System Integration</u>	
11:45	<b>Mechatronic System Integration of the Hybrid Powertrain</b> Y. Tadros, T. Harder, ECPE
12:15	Lunch
13:30	<b>Mechatronic System Integration in Aerospace (More-Electric-Aircraft)</b> R. Meuret, Hispano-Suiza
14:00	<b>Mechatronic System Integration in Industrial Drives</b> J. Popovic-Gerber, ECPE/TU Delft
14:30	Coffee break
<u>Reliability</u>	
15:00	<b>High Temperature and Harsh Environment</b> G. Coquery, INRETS
15:30	<b>Reliability of Ag Sintering vs. Soldering</b> R. Eisele, University of Applied Science Kiel (invited)
16:00	Wrap up and Discussion
16:15	End of workshop