

TECHNICAL PROGRAM

Opening Remarks

Monday, June 7, 9:00-9:15

Y. Seki, *Fuji Electric Systems*

Plenary Session 1

Monday, June 7, 9:15-10:00

Chairperson: Y. Seki, *Fuji Electric Systems*

M. Darwish, *MaxPower Semiconductor*

1. Solarpower(tentative)

O. Stalter

Fraunhofer-Institute, Germany

Plenary Session 2

Monday, June 7, 10:20-11:50

Chairperson: G. Majumdar, *Mitsubishi Electric*

M. Mori, *Hitachi*

1. AutomotiveElectronics(tentative)

Y. Yamamoto

Honda, Japan

2. An European state-of-the-art "green power electronics technology" evolution like a windpower

R. W. de Doncker

RWTH Aachen, Germany

Session 1: High Voltage Power Devices I

Monday, June 7, 13:10-14:25

Chairperson: K. Satoh, *Mitsubishi Electric*

S. Linoler, *ABB Switzerland*

1-1 Deep melt activation using laser thermal annealing for IGBT thin wafer technology

T. Gutt and H. Schulze*

*Infineon Technologies, Germany and *Infineon Technologies, Austria*

1-2 Failure mechanism and improvement potential of IGBT's short circuit operation

F. Hille, F. Umbach, T. Raker and R. Roth*

*Infineon Technologies, Germany and *Infineon Technologies, Austria*

1-3 Ultra High Speed Short Circuit Protection for IGBT with Gate Charge Sensing

K. Yuasa, S. Nakamichi and I. Omura

Kyushu Institute of Technology, Japan

Session 2: Module and Package Technologies

Monday, June 7, 14:45-16:00

Chairperson: K. Hamada, *Toyota Motor*

D. Silber, *University of Bremen*

2-1 Development of New Power Control Unit for Compact-Class Vehicle

S. Nozawa, T. Maekawa, E. Yagi, Y. Terao and H. Kohno

Toyota Motor, Japan

- 2-2 Simple, Compact, Robust, and High-performance Power module T-PM (Transfer-molded Power Module)**
 T. Ueda, N. Yoshimatsu*, N. Kimoto*, D. Nakajima, M. Kikuchi and T. Shinohara
*Mitsubishi Electric and *Fukuryo Semicon Engineering, Japan*
- 2-3 Package Level Integration of a Monolithic Buck Converter Power IC and Bondwire Magnetics**
 H. Jia, J. Lu and Z. John Shen
University of Central Florida, USA

Session 3: Power ICs I

Monday, June 7, 16:10-17:25

Chairperson: T. Terashima, *Mitsubishi Electric*

R. Zhu, *Freescale Semiconductor*

- 3-1 An Integrated DC-DC Converter with One-Step Digital Dead-time Correction**
 A. Y. Zhao, A. Shorten, H. Nishio* and W. Tung Ng
*University of Toronto, Canada and *Fuji Electric Holdings, Japan*
- 3-2 Towards a Universal Model for Hot Carrier Degradation in DMOS Transistors**
 P. Moens, D. Varghese* and M. Alam*
*ON Semiconductor, Belgium and *Purdue University, USA*
- 3-3 Application of GaAs pHEMT Technology for Efficient High Frequency Switching Regulators**
 V. Pala, H. Peng, M.M. Hella and T.P. Chow
Rensselaer Polytechnic Institute, USA

Session 4: Power ICs II

Tuesday, June 8, 8:30-10:10

Chairperson: D. Disney, *Monolithic Power Systems*

S. Pendharkar, *Texas Instruments*

- 4-1 BD180LV – 0.18 μm BCD Technology with Best-in-Class LDMOS from 7V to 30V**
 K.-Y. Ko, I.-Y. Park, Y.-K. Choi, C.-J. Yoon, J.-H. Moon, K.-M. Park, H.-C. Lim, S.-Y. Park, N.-J. Kim and K.-D. Yoo
Dongbu HiTek, Korea
- 4-2 A 120V 180nm High Voltage CMOS smart power technology for System-on-chip integration**
 Minixhofer, Feilchenfeld*, Knaipp, Röhrer, Park, Zierak*, Enichlmair, Levy*, Löffler, Hershberger*, Unterleitner, Gautsch*, Chatty*, Shi*, Posch, Seebacher, Schrems, Dunn* and Haramé*
*austriamicrosystems, Austria and *IBM, USA*
- 4-3 A High Voltage Super-Junction NLD MOS Device Implemented in 0.13 μm SOI Based Smart Power IC Technology**
 R. Zhu, V. Khemka, T. Khan, W. Huang, X. Cheng, P. Hui, M. Ger and P. Rodriguez
Freescale Semiconductor, USA
- 4-4 Large Current Capability 270V Lateral IGBT with Multi-Emitter**
 J. Sakano, S. Shirakawa, K. Hara, S. Yabuki, S. Wada, J. Noguchi and M. Wada
Hitachi, Japan

Session 5: Power ICs III

Tuesday, June 8, 10:30-12:10

Chairperson: J. Sin, *Hong Kong University of Science and Technology*
S. Banerjee, *Power Integrations*

- 5-1 Using multiplication to evaluate HCI degradation in HV-SOI devices**
R. van Dalen, P.W.M. Boos, A.B. van der Wal, M.J. Swanenberg and A. Heringa*
*NXP, The Netherlands and *High Voltage NXP research, Belgium*
- 5-2 A new 1200V HVIC with a novel high voltage Pch-MOS**
M. Yoshino, K. Shimizu and T. Terashima
Mitsubishi Electric Corporation
- 5-3 Integration of 1200V SOI gate driver ICs into a medium power IGBT module package**
B. Vogler, M. Rossberg, R. Herzer and L. Reusser
SEMIKRON Elektronik, Germany
- 5-4 A Novel 600V-LDMOS with HV-Interconnection for HVIC on Thick SOI**
M. Yamaji, K. Abe*, T. Maiguma*, H. Takahashi* and H. Sumida
*Fuji Electric Holdings, Japan and *Fuji Electric Systems, Japan*

Session 6: High Voltage Power Devices II

Tuesday, June 8, 13:30-15:10

Chairperson: D Pattanayak, *Vishay Siliconix*
J. L. Sanchee, *LAAS-CNRS*

- 6-1 Design of Trench Termination for High Voltage Devices**
R. Kamibaba, K. Takahama and I. Omura
Kyushu Institute of Technology, Japan
- 6-2 A concept of novel edge termination technique: Recess Junction Termination (RJT)**
S. Honda, R. Fujii*, T. Kawakami**, S. Fujioka***, A. Narazaki and K. Motonami
*Mitsubishi Electric, Japan, *Organization of Manufacturing Engineering Center, Japan, **Advanced Technology R&D Center, Japan and ***Renesas Semiconductor Engineering, Japan*
- 6-3 Inhibiting Effect of Middle Broad Buffer Layer Diode Using Hydrogen- Related Shallow Donor on Reverse Recovery Oscillation**
T. Mizushima, M. Nemoto*, H. Kuribayashi**, T. Yoshimura** and H. Nakazawa
*Fuji Electric Holdings, Japan *Fuji Technosurvey, Japan and **Fuji Electric Systems, Japan*
- 6-4 Challenge to the Barrier of Conduction Loss in PiN Diode toward $V_F < 300$ mV with pulsed carrier injection concept**
Y. Matumoto, K. Takahama, and I. Omura
Kyushu Institute of Technology, Japan

Poster Session

Tuesday, June 8, 15:30-17:30

- HV-P1 Simulation of Cosmic Ray Failures Rates using Semiempirical Models**
F. Pfirsch and G. Soelkner
Infineon Technologies, Germany

- HV-P2 Cosmic Ray Ruggedness of IGBT for Hybrid Vehicles**
S. Nishida, T. Ohnishi, N. Nose, T. Fujikawa, K. Hamada, T. Shoji* and M. Ishiko*
*Toyota Motor, Japan and *Toyota Central R&D Labs., Japan*
- HV-P3 Advanced RFC Technology Having New Cathode Structure of Field Limiting Rings Region for High Voltage Planar Diode**
K. Nakamura, F. Masuoka, A. Nishii, K. Sadamatsu, S. Kitajima and K. Hatade
Mitsubishi Electric, Japan
- HV-P4 Investigations of Inhomogeneous Operation of IGBTs Under Unclamped Inductive Switching Condition**
Y. Mizuno, R. Tagami and K. Nishiwaki
Toyota Motor, Japan
- HV-P5 Optimization of the temperature dependence of the anode-side current gain of IGBTs by field-stop design**
S. Voss, H.-J. Schulze and F.-J. Niedernostheide
Infineon Technologies, Germany
- HV-P6 Carrier Lifetime Control Optimization for High Speed IGBT Based on Electrical and Physical Analysis**
C. Tadokoro, M. Kaneda, A. Kiyoi, S. Kusunoki and H. Kurokawa*
Mitsubishi Electric, Japan
- HV-P7 Reverse-conducting Insulated Gate Bipolar Transistor with an Anti-parallel Thyristor**
W. C.-W. Hsu, F. Udrea, H.-Y. Hsu* and W.-C. Lin*
*University of Cambridge, UK and *Anpec Electronics, Taiwan*
- HV-P8 A new way to alleviate the RC IGBT snapback phenomenon: The SuperJunction Solution**
M. Antoniou, F. Udrea, F. Bauer* and I. Nistor*
*University of Cambridge, UK and *ABB Switzerland, Switzerland*
- HV-P9 BJT application expansion by insertion of Superjunction**
L. Théolier, C. Benboujema, A. Schellmanns, N. Batut, Y. Raingeaud and J.-B. Quoirin*
*Université François Rabelais, France and *ST Microelectronics, France*
- HV-P10 Free Carrier Absorption Investigations on ion Irradiated Fast Recovery Diodes**
X. Perpiñà, X. Jordà, M. Vellvehi, J. Vobecky* and J. Millán
*Centro Nacional de Microelectrónica, Spain and *Czech Technical University in Prague, Czech Republic*
- HV-P11 A new diode structure with Inverse injection Dependency of Emitter Efficiency**
R. Baburske, J. Lutz, H. Schulze* and R. Siemieniec**
*Chemnitz University of Technology, Germany, *Infineon Technologies, Germany and **Infineon Technologies, Austria*
- HV-P12 Numerical study on very high speed silicon PiN diode possibility for power ICs in comparison with SiC-SBD**
K. Takahama and I. Omura
Kyusyu Institute of Technology, Japan

- LV-P1 Analysis of technological concerns on electrical characteristics of 0.18 μ m SOI power LUDMOS transistors**
 G. Toulon^{*,**}, I. Cortés^{*,**}, F. Morancho^{*,**}, E. Hugonnard-Bruyere^{***}, B. Villard^{***} and W. J. Toren^{***}
CNRS, France, **Université de Toulouse, France and *ATMEL Rousset, France*
- LV-P2 Low Vgs P-ch LDMOS with Sallow Pwell from 8V to 60V**
 C.-J. Ko, C.-H. Cho, H.-B. Lee, Y.-J. Lee, M.-W. Kim, S.-K. Bang, H.-G. Kim, S.-C. Shim, N.-J. Kim and K.-D. Yoo
Dongbu Hitek, Korea
- LV-P3 Reduced on-resistance in LDMOS devices by integrating trench gates into planar technology**
 T. Erlbacher, A. J. Bauer and L. Frey
Fraunhofer Institute, Germany
- LV-P4 Numerical Simulation of Metal Interconnects of Power Semiconductor Devices**
 M. Ershov, A. Tcherniaev, Y. Feinberg, P. Lindorfer^{*}, Wi. French^{*} and P. Hopper^{*}
*Silicon Frontline Technology, USA and *National Semiconductor, USA*
- LV-P5 Simulation of Off-State degradation at high temperature in High Voltage NMOS transistor with STI architecture**
 S. Bach, S. Manzini, J. Cambieri, G. Pizzo, A. Causio, L. Atzeni, D. Riccardi, L. Zullino, G. Croce and A. Nannipieri^{*}
*STMicroelectronics, Italy and *Synopsys Switzerland LLC, Switzerland*
- LV-P6 Analysis of Double Hump Substrate Current in NLD MOSFET**
 R.Y. Su, K.Y. Tai and J. Gong
National Tsing Hua University, Taiwan
- LV-P7 On the Quasi-Saturation Behavior of a Novel Vertical Power MOSFET with Self-Aligned Gate**
 W. Z. Cai, B. P. Gogoi, R. B. Davies and D. Lutz
HVVi Semiconductors, USA
- LV-P8 A Novel Low-Voltage Trench Power MOSFET with Improved Avalanche Capability**
 J. C. W. Ng, J. K. O. Sin, H. Sumida^{*}, Y. Toyoda^{*}, A. Ohi^{**}, H. Tanaka^{**}, T. Nishimura^{**} and K. Ueno^{*}
*Hong Kong University of Science and Technology Clear Water Bay, Hong Kong, *Fuji Electric Holdings, Japan and **Fuji Electric Systems, Japan*
- LV-P9 Analytical calculation of the breakdown voltage for balanced, symmetrical superjunction power devices**
 E. Napoli, H. Wang^{*} and F. Udrea^{**}
*University of Napoli Federico II, Italy, *MIT, USA and **University of Cambridge, UK*
- LV-P10 Power MOSFETs' Operation in Cryogenic Temperatures: Comparison between HEXFETR, MDMeshTM and CoolMOSTM**
 K.K. Leong, A.T. Bryant and P.A. Mawby
University of Warwick, UK

- NM-P1 Development of 6kV-class SiC-PiN diodes for high-voltage power inverter**
Y. Tanaka, K. Takao*, K. M. Sung**, K. Wada***, T. Kanai**** and H. Ohashi
*AIST, Japan, *Toshiba, Japan, **Ibaraki National College of Technology, Japan, ***Tokyo Metropolitan University, Japan and ****Toshiba Mitsubishi-Electric Industrial Systems, Japan*
- NM-P2 A Novel 4H-SiC IGBT Structure with Improved Trade-off between Short Circuit Capability and On-state Voltage Drop**
W. Sung, A. Q. H. and B. J. Baliga
North Carolina State University, USA
- NM-P3 Channel Scaling of Hybrid GaN MOS-HEMTs**
Z. Li and T. P. Chow
Rensselaer Polytechnic Institute, USA
- NM-P4 Experimental Study on Current Collapse of GaN MOSFETs, HEMTs and MOS-HEMTs**
Z. Li, T. Marron, H. Naik, W. Huang and T. P. Chow
Rensselaer Polytechnic Institute, USA
- NM-P5 Normally-off operation of Al₂O₃/GaN MOSFET based on AlGaIn/GaN heterostructure with p-GaN buffer layer**
D.-S. Kim, S.-N. Kim, E.-H. Kwak, S.-G. Lee, H.-S. Kang, J.-S. Lee, K.-S. Im, K.-W. Kim, J.-B. Ha and J.-H. Lee
Kyungpook National University, Korea
- NM-P6 High Voltage AlGaIn/GaN HEMTs Employing Oxygen Annealing**
Y.-H. Choi, J. Lim, Y.-S. Kim, O. Seok and M.-K. Han
Seoul National University, Korea
- NM-P7 Breakdown Voltage Enhancement for GaN High Electron Mobility Transistors**
G. Xie, B. Zhang* and W.T. Ng
*University of Toronto, Canada and *University of Electronic science and Technology of China, China*
- IC-P1 Power LDMOS with Novel STI Profile for Improved Rsp, BVDSS, and Reliability**
S. Haynie, A. Gabrys, T. Kwon, P. Allard, J. Strout and A. Strachan
National Semiconductor, USA
- IC-P2 A New 8V – 60V rated Low Vgs NLD MOS Structure with Enhanced Specific on-Resistance**
C.-J. Ko, C.-H. Cho, H.-B. Lee, Y.-J. Lee, M.-W. Kim, S.-K. Bang, H.-G. Kim, J.-O Lee, S.-C. Shim, N.-J. Kim and K.-D. Yoo
Dongbu Hitek, Korea
- IC-P3 Cost-Effective High-Voltage Drain Extended PMOS Integration in an advanced STI LBC Technology**
M. Denison, M.-Y. Chuang, S. Merchant, S. Pendharkar, B. Hu, Q. Wang, J. Lin, B. Wofford, Y. Zhang and J. Arch
Texas Instruments, USA
- IC-P4 Enhancement of Current Drivability in Field PMOS by Optimized Field Plate**
S. Tokumitsu, T. Nitta, T. Shiromoto, T. Kuroi, K. Hatasako and S. Maegawa
Renesas Technology, Japan

- IC-P5 A 200V Partial SOI 0.18 μ m BCD technology**
A. Hölke, D. K. Pal, Y. Hao, K. K. Yaw, E. Kho, G. Kittler*, U. Kuniss* and J. Gessner*
*X-Fab Sarawak, Malaysia and *X-Fab Semiconductor Foundries, Germany*
- IC-P6 Analysis of Transient Characteristics of Lateral-IGBT/Diode in Silicon on Insulator Characterized by Trenched Buried Oxide Structure**
S. Shiraki, Y. Ashida, S. Takahashi and N. Tokura
DENSO, Japan
- IC-P7 A Novel High Voltage (>700V) SOI LDMOS with Buried N-layer in a Selfisolation High Voltage Integrated Circuit**
X. Luo, T. Lei, W. Yuangang, B. Zhang and F. Udrea*
*University of Electronic Science and Technology of China, China and *University of Cambridge, UK*
- IC-P8 Design of Highly Stable 700V Lateral RESURF MOSFETs For New Generation Low- Cost, Highly Efficient, Off-line Switching-mode Power Supplies**
S. Banerjee, V. Parthasarathy and M. Manley
Power Integrations, USA
- IC-P9 Demonstration of MHz-Frequency Operation of a Monolithic Self-Synchronized Rectifier IC in Flyback DC/DC Converters**
H. Jia, O. Abdel-Rahman, I. Batarseh and Z. J. Shen
University of Central Florida, USA
- IC-P10 Digitally Controlled Integrated DC-DC Converter with Transient Suppression**
J. Wang, K. Ng, T. Kawashima*, M. Sasaki*, H. Nishio*, A. Prodić and W.T. Ng
*University of Toronto, Canada and *Fuji Electric Holdings, Japan*
- IC-P11 Second-Generation One Chip Li-ion Battery Protection IC With an Asymmetric Bidirectional Trench Lateral Power MOSFET**
M. Sawada, H. Arai*, H. Takahashi*, A. Kitamura*, G. Tada* and N. Fujishima*
*Fuji Electric Holdings, Japan and *Fuji Electric Systems, Japan*
- IC-P12 In situ Defect-Screening of Integrated LDMOS for Critical Automotive Applications**
V. Malandrucolo, M. Ciappa, H. Rothleitner* and W. Fichtner
*Swiss Federal Institute of Technology, Switzerland and *Infineon Technologies, Austria*
- MP-P1 A study of the bonding-wire reliability on the chip surface electrode in IGBT**
Y. Ikeda, H. Hokazono, S. Sakai* and Y. Takahashi
*Fuji Electric Holdings, Japan and *Fuji Electric Systems, Japan*
- MP-P2 Development of ultrasonic welding for IGBT module structure**
Y. Nishimura, K. Kido, F. Momose and T. Goto
Fuji Electric Systems, Japan
- MP-P3 A Computationally Efficient Electro-Thermal Modelling Technique for Coupled Multi-Disciplinary Analysis of Multi-Chip Power Modules**
P. Evans, A. Castellazzi, F. Carastro and C M. Johnson
University of Nottingham, UK

Session 7: Low Voltage Power Devices I

Wednesday, June 9, 8:30-10:10

Chairperson: S. Matsumoto, *NTT*

J. Sonsky, *NXP Semiconductors*

7-1 The Influence of The Layout On The ESD Performance Of HV-LDMOS

J.-H. Lee, H.-D. Su*, DH Yang**, J. F. Chen** and KM Wu*

*R&D/TSMC, Canada, *Richtek Technology, Taiwan and **R&D/TSMC, Taiwan*

7-2 Improving Surface Bipolar Activity in Thin Gate Oxide De-nmos – A Critical HV I/O ESD Protection Element For Nanometer Scale Technologies

A. Chatterjee, S. Pendharkar* and C. Duvvury*

*University of California, USA and *Texas Instruments, USA*

7-3 Investigation on the temperature dependence of the HCI effects in the rugged STI-based LDMOS transistor

S. Poli, S. Reggiani, M. Denison, G. Baccarani, E. Gnani, A. Gnudi, S. Pendharkar*, R. Wise* and S. Seetharaman*

*University of Bologna, Italy and *Texas Instruments, USA*

7-4 0.13 μ m CMOS/DMOS platform technology with novel 8V/9V LDMOS for low voltage high-frequency DC-DC converters

T. Matsudai, K. Sato, K. Endo and N. Yasuhara

Toshiba, Japan

Session 8: Low Voltage Power Devices II

Wednesday, June 9, 10:30-12:10

Chairperson: Y. Kawaguchi, *Toshiba*

M. Darwish, *MaxPower Semiconductor*

8-1 Analyzing Super-Junction C-V to Estimate Charge Imbalance

M. Bobde, L. Guan, A. Bhalla, F. Wang and M. Ho

Alpha & Omega Semiconductor, USA

8-2 Low Voltage TrenchMOS combining low specific RDS(on) and QG FOM

P. Rutter and S. Peake

NXP Semiconductors, UK

8-3 Narrow-Pitch Superjunction UMOSFET Fabricated by Multiple Ion Implantations for 40V-Class Automotive Application

Y. Kawashima, K. Murakawa and Y. Miura

NEC Electronics, Japan

8-4 Optimizing Oxide Charge Balanced Devices for Unclamped Inductive Switching (UIS)

J. Yedinak, D. Probst, G. Dolny, A. Challa and J. Andrews

Fairchild Semiconductor, USA

Session 9: New Material Power Devices I

Wednesday, June 9, 13:30-15:10

Chairperson: N. Ikeda, *Advanced Power Device R&D association*

P. Moens, *ON Semiconductor*

9-1 Influence of Electric Field upon Current Collapse Phenomena and Reliability in High Voltage GaN-HEMTs

W. Saito, T. Nitta, Y. Kakiuchi, Y. Saito, T. Noda, H. Fujimoto, A. Yoshioka and T. Ohno

Toshiba, Japan

9-2 Self-Protected GaN Power Devices with Reverse Conduction Blocking and Forward Current Limiting Capabilities

C. Zhou, W. Chen, E. L. Piner* and K. J. Chen

Hong Kong University of Science and Technology, Hong Kong and

**Nitronex, USA*

9-3 Normally-off AlGaIn/GaN HFET with p-type GaN Gate and AlGaIn Buffer

O. Hilt, A. Knauer, F. Brunner, E. Bahat-Treidel and J. Wurfl

Ferdinand-Braun-Institut, Germany

9-4 Long Term Stability of Packaged SiC Schottky Diodes in the -170°C/+280°C Temperature Range

P. Godignon, X. Jorda, V. Banu, M. Vellvehi, J. Millan, P. Brosseard*, D. Lopez** and J. Barbero**

*CNM (CSIC), Spain, *Laboratoire Ampere, France and **ALTER Technology, Spain*

Session 10: New Material Power Devices II

Wednesday, June 9, 15:30-17:10

Chairperson: N. Iwamura, *AIST*

D. Sheridan, *SemiSouth*

10-1 1200 V, 35 A SiC-BGSIT with improved blocking gain of 480

Y. Tanaka, A. Takatsuka*, K. Yano*, T. Yatsuo and K. Arai**

*AIST, Japan and *Yamanashi University, Japan*

10-2 Saturation Current Improvement in 1200 V Normally-Off SiC VJFETs using Non-Uniform Channel Doping

A. Ritenour, D.C. Sheridan, V. Bondarenko and J.B. Casady

SemiSouth, USA

10-3 1400 Volt, 5 mΩ-cm² SiC MOSFETs for High-Speed Switching

K. Matocha, P. Losee, S. Arthur, J. Nasadoski, J. Glaser, G. Dunne and L. Stevanovic

GE Global Research Center, USA

10-4 High Surge Current Ruggedness of 5kV class 4H-SiC SiCGT

S. Ogata, K. Asano, Y. Sugawara*, A. Tanaka, Y. Miyanagi, K. Nakayama, T. Izumi, T. Hayashi and M. Nishimura

*The Kansai Electric Power, Japan and *SiC power electronics network, Japan*

Panel Discussion

Wednesday, June 9, 17:30-19:00

Chairperson:

Prospects of WBG Devices

Session 11: High Voltage Power Devices III

Thursday, June 10, 8:30-10:10

Chairperson: I. Omura, *Kyushu Institute of Technology*

R. Herzer, *Semikron Elektronik*

11-1 A 600V Super Low Loss IGBT with Advanced Micro-P Structure for the Next Generation IPM

M. Momose, K. Kumada, H. Wakimoto*, Y. Onozawa, A. Nakamori, K. Sekigawa, M. Watanabe, T. Yamazaki and N. Fujishima

*Fuji Electric Systems, Japan and *Fuji Electric Holdings, Japan*

11-2 DB (Dielectric Barrier)-IGBT with Extreme Injection Enhancement

M. Takei, T. Naito, T. Kawashima and H. Nakazawa

Fuji Electric Holdings, Japan

11-3 Wide Cell Pitch LPT(II)-CSTBTM(III) Technology Rating up to 6500V for Low Loss

K. Nakamura, K. Sadamatsu, D. Oya, H. Shigeoka* and K. Hatade*

*Mitsubishi Electric, Japan and *Fukuryo Semicon Engineering, Japan*

11-4 A comparison of charge dynamics in the Reverse-Conducting RC-IGBT and Bi-mode Insulated Gate Transistor BIGT

L. Storasta, A. Kopta and M. Rahimo

ABB Switzerland, Switzerland

Session 12: Low Voltage Power Devices III

Thursday, June 10, 10:30-11:45

Chairperson: K. Kobayashi, *NEC Electronics*

V. Khemka, *Freescale Semiconductor*

12-1 New VDMOS Structure with Discontinuous Thick Inter-Body Oxide to Reduce Gate-to-Drain Charge

J. Roig, S. Mouhoubi, P. Gassot, R. Charavel, A. Suvkhanov*, P. Moens, F. Bauwens and M. Tack

*ON Semiconductor, Belgium and *ON Semiconductor, USA*

12-2 A study of p stopper effect on 30V-gate/80V-drain bi-directional NMOSFET and 80V ESD protection BJT

H. Fujii, S. Komatsu, M. Sato and T. Ichikawa

NEC Electronics, Japan

12-3 A New P-channel Bidirectional Trench Power MOSFET for Battery Charging and Protection

F. Robb, A. Ball and K. Huang*

ON Semiconductor, USA

Award & Closing

Thursday, June 10, 11:45-12:15

Chairperson: Y. Seki, *Fuji Electric*

G. Majumdar, *Mitsubishi Electric*

M. Mori, *Hitachi*

M. Darwish, *MaxPower Semiconductor*